AiP74LVC2T45-Q1
2-bit Dual Supply Translating Transceiver; 3-State

Product Specification

Specification Revision History:

Version	Date	Description
2022-06-A1	2022-06	New

Contents

1、General Description

The AiP74LVC2T45-Q1 is dual bit, dual supply translating transceiver with 3-state outputs that enable bidirectional level translation. The device suitable for translating between any of the low voltage nodes (1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V).

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

Features:

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
- Wide supply voltage range:
  $V_{CC(A)}$: 1.2V to 5.5V
  $V_{CC(B)}$: 1.2V to 5.5V
- ±24mA output drive (V_{CC}=3.0V)
- Inputs accept voltages up to 5.5V
- Low power consumption
- High-impedance when $V_{CC(A)}$ or $V_{CC(B)}$ =0V
- ESD-HBM:3000V(AEC-Q100-002)
- ESD-CDM:All pins 750V (AEC-Q100-011)
- LATCH-UP: ±100mA,T_{amb}=125℃(AEC-Q100-004)
- Temperature range:-40℃ to +125℃
- Packaging information:VSSOP8

Ordering Information:

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVC2T45-Q1 YA8.TR	VSSOP8	CIQXX	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 2.0mm×2.3mm Pin spacing: 0.50mm

Note 1: "XX" refers to variable content, meaning year and package batch serial number.

Note 2: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

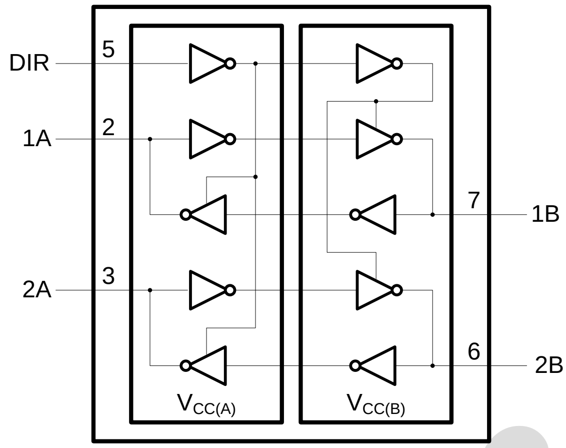


Figure 1. Logic diagram

2.2、Pin Configurations

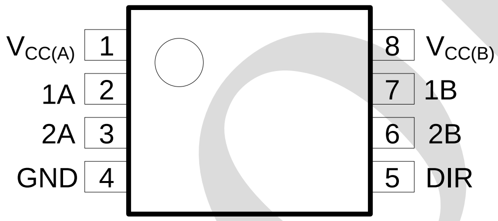


Figure 2. Pin Configurations

2.3、Pin Description

Pin No.	Pin Name	Description
1	$V_{CC(A)}$	supply voltage A (port A and DIR)
2	1A	data input or output
3	2A	data input or output
4	GND	ground (0V)
5	DIR	direction control
6	2B	data input or output
7	1B	data input or output
8	$V_{CC(B)}$	supply voltage B (port B)

2.4、Function Table[1]

Supply Voltage	Input	Input/output[2]	
$V_{CC(A)}$, $V_{CC(B)}$	DIR	nA	nB
1.2V to 5.5V	L	nA=nB	input
1.2V to 5.5V	H	input	nB=nA
GND[3]	X	Z	Z

Note:

[1] H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	-0.5	+6.5	V
supply voltage B	$V_{CC(B)}$	-	-0.5	+6.5	V
supply current	I_{CC}	$I_{CC(A)}$ or $I_{CC(B)}$; per V_{CC} pin	-	100	mA
ground current	I_{GND}	-	-100	-	mA
input voltage	V_I	-	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output voltage	V_O	Active mode	-0.5	V_{CCO}+0.5	V
		Suspend mode	-0.5	+6.5	V
output current	I_O	V_O=0V to V_{CCO}	-	±50	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
soldering temperature	T_L	10s	260		℃

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage A	$V_{CC(A)}$	-	1.2	-	5.5	V
supply voltage B	$V_{CC(B)}$	-	1.2	-	5.5	V
input voltage	V_I	-	0	-	5.5	V
ambient temperature	T_{amb}	-	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	V_{IH}	data input[1]	V_{CCI}=1.2V	0.8V_{CCI}	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65V_{CCI}	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7V_{CCI}	-	-	V
		DIR input	V_{CCI}=1.2V	0.8$V_{CC(A)}$	-	-	V
			V_{CCI}=1.4V to 1.95V	0.65$V_{CC(A)}$	-	-	V
			V_{CCI}=2.3V to 2.7V	1.7	-	-	V
			V_{CCI}=3.0V to 3.6V	2.0	-	-	V
			V_{CCI}=4.5V to 5.5V	0.7$V_{CC(A)}$	-	-	V
LOW-level input voltage	V_{IL}	data input[1]	V_{CCI}=1.2V	-	-	0.2V_{CCI}	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35V_{CCI}	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3V_{CCI}	V
		DIR input	V_{CCI}=1.2V	-	-	0.2$V_{CC(A)}$	V
			V_{CCI}=1.4V to 1.95V	-	-	0.35$V_{CC(A)}$	V
			V_{CCI}=2.3V to 2.7V	-	-	0.7	V
			V_{CCI}=3.0V to 3.6V	-	-	0.8	V
			V_{CCI}=4.5V to 5.5V	-	-	0.3$V_{CC(A)}$	V
HIGH-level output voltage	V_{OH}	V_I=V_{IH}	I_O=-100uA; V_{CCO}=1.2V to 4.5V[2]	V_{CCO}-0.1	-	-	V
			I_O=-6mA; V_{CCO}=1.4V	1.0	-	-	V
			I_O=-8mA; V_{CCO}=1.65V	1.2	-	-	V
			I_O=-12mA; V_{CCO}=2.3V	1.9	-	-	V
			I_O=-24mA; V_{CCO}=3.0V	2.4	-	-	V
			I_O=-32mA; V_{CCO}=4.5V	3.8	-	-	V
LOW-level output voltage	V_{OL}	V_I=V_{IH}[2]	I_O=100uA; V_{CCO}=1.2V to 4.5V	-	-	0.1	V
			I_O=6mA; V_{CCO}=1.4V	-	-	0.3	V
			I_O=8mA; V_{CCO}=1.65V	-	-	0.45	V
			I_O=12mA; V_{CCO}=2.3V	-	-	0.3	V
			I_O=24mA; V_{CCO}=3.0V	-	-	0.55	V
			I_O=32mA; V_{CCO}=4.5V	-	-	0.55	V
input leakage current	I_I	DIR input; V_I=0V to 5.5V; V_{CCI}=1.2V to 5.5V		-	-	±10	uA
OFF-state output	I_{OZ}	A or B port; V_O=0V or V_{CCO}; V_{CCO}=1.2V to 5.5V[2]		-	-	±10	uA
power-off leakage	I_{OFF}	A port; V_I or V_O=0V to 5.5V; $V_{CC(A)}$=0V; $V_{CC(B)}$=1.2V to 5.5V		-	-	±10	uA

current		B port; V_I or V_O=0V to 5.5V; $V_{CC(B)}$=0V; $V_{CC(A)}$=1.2V to 5.5V		-	-	±10	uA
supply current	I_{CC}	A port; V_I=0V or V_{CCI}; I_O=0A[1]	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(A)}$=5.5V; $V_{CC(B)}$=0V	-	-	2	uA
			$V_{CC(A)}$=0V; $V_{CC(B)}$=5.5V	-2	-	-	uA
		B port; V_I=0V or V_{CCI}; I_O=0A	$V_{CC(A)}$, $V_{CC(B)}$=1.2V to 5.5V	-	-	8	uA
			$V_{CC(A)}$, $V_{CC(B)}$=1.65V to 5.5V	-	-	3	uA
			$V_{CC(B)}$=0V; $V_{CC(A)}$=5.5V	-2	-	-	uA
			$V_{CC(B)}$=5.5V; $V_{CC(A)}$=0V	-	-	2	uA
additional supply current	ΔI_{CC}	per input; $V_{CC(A)}$, $V_{CC(B)}$= 3.0V to 5.5V	A port; A port at $V_{CC(A)}$-0.6V; DIR at $V_{CC(A)}$; B port=open	-	-	75	uA
			DIR input; DIR at $V_{CC(A)}$-0.6V; A port at $V_{CC(A)}$ or GND; B port=open	-	-	75	uA
			B port; B port at $V_{CC(B)}$-0.6V; DIR at GND; A port=open	-	-	75	uA

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

3.3.2、AC Characteristics

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified)

Parameter	**Symbol**	**Conditions**	**$V_{CC(B)}$**										**Unit**
			1.5V±0.1V		**1.8V±0.15V**		**2.5V±0.2V**		**3.3V±0.3V**		**5.0V±0.5V**		
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
$V_{CC(A)}$=1.4V to 1.6V													
LOW to HIGH propagation delay	t_{PLH}	nA to nB	-	24.2	-	20.0	-	15.1	-	13.2	-	11.8	ns
		nB to nA	-	24.2	-	21.4	-	17.8	-	17.5	-	17.1	ns
HIGH to LOW propagation delay	t_{PHL}	nA to nB	-	21.7	-	17.2	-	13.3	-	12.2	-	11.9	ns
		nB to nA	-	21.7	-	19.4	-	14.9	-	12.7	-	12.3	ns
HIGH to OFF-state propagation delay	t_{PHZ}	DIR to nA	-	21.1	-	21.1	-	21.1	-	21.1	-	21.1	ns
		DIR to nB	-	27.5	-	26.2	-	15.5	-	14.5	-	13.8	ns
LOW to OFF-state propagation delay	t_{PLZ}	DIR to nA	-	12.9	-	12.9	-	12.9	-	12.9	-	12.9	ns
		DIR to nB	-	20.4	-	19.3	-	14.5	-	13.6	-	12.8	ns
OFF-state to HIGH propagation delay	t_{PZH}	DIR to nA	-	43.7	-	40.4	-	27.3	-	25.3	-	24.0	ns
		DIR to nB	-	36.3	-	32.4	-	27.8	-	25.6	-	24.5	ns

OFF-state to LOW propagation delay	t_{PZL}	DIR to nA	-	48.9	-	45.3	-	27.1	-	25.2	-	23.8	ns
		DIR to nB	-	42.1	-	38.2	-	34.2	-	33.2	-	32.8	ns
$V_{CC(A)}$=1.65V to 1.95V													
LOW to HIGH propagation delay	t_{PLH}	nA to nB	-	21.4	-	19.9	-	10.7	-	8.5	-	7.9	ns
		nB to nA	-	20.1	-	19.9	-	16.7	-	13.9	-	13.4	ns
HIGH to LOW propagation delay	t_{PHL}	nA to nB	-	19.1	-	15.8	-	9.9	-	8.3	-	8.0	ns
		nB to nA	-	17.2	-	15.8	-	14.5	-	14.2	-	13.7	ns
HIGH to OFF-state propagation delay	t_{PHZ}	DIR to nA	-	19.2	-	19.2	-	19.2	-	19.2	-	19.2	ns
		DIR to nB	-	26.9	-	24.5	-	14.1	-	13.2	-	11.5	ns
LOW to OFF-state propagation delay	t_{PLZ}	DIR to nA	-	12.2	-	12.2	-	12.2	-	12.2	-	12.2	ns
		DIR to nB	-	20.2	-	18.6	-	12.4	-	11.5	-	10.4	ns
OFF-state to HIGH propagation delay	t_{PZH}	DIR to nA	-	39.2	-	37.3	-	28.2	-	26.8	-	24.5	ns
		DIR to nB	-	33.0	-	31.4	-	22.3	-	19.9	-	19.3	ns
OFF-state to LOW propagation delay	t_{PZL}	DIR to nA	-	43.8	-	40.2	-	27.3	-	25.6	-	22.7	ns
		DIR to nB	-	38.5	-	35.1	-	28.6	-	27.1	-	26.9	ns
$V_{CC(A)}$=2.3V to 2.7V													
LOW to HIGH propagation delay	t_{PLH}	nA to nB	-	19.9	-	17.7	-	9.6	-	7.1	-	5.5	ns
		nB to nA	-	15.1	-	10.1	-	9.6	-	8.6	-	8.3	ns
HIGH to LOW propagation delay	t_{PHL}	nA to nB	-	17.5	-	14.5	-	8.4	-	6.5	-	5.4	ns
		nB to nA	-	13.5	-	9.6	-	8.4	-	7.7	-	6.8	ns
HIGH to OFF-state propagation delay	t_{PHZ}	DIR to nA	-	9.0	-	9.0	-	9.0	-	9.0	-	9.0	ns
		DIR to nB	-	24.8	-	23.8	-	12.3	-	10.1	-	9.1	ns
LOW to OFF-state propagation delay	t_{PLZ}	DIR to nA	-	6.8	-	6.8	-	6.8	-	6.8	-	6.8	ns
		DIR to nB	-	16.1	-	14.6	-	10.1	-	9.6	-	8.5	ns
OFF-state to HIGH propagation delay	t_{PZH}	DIR to nA	-	30.5	-	24.5	-	18.9	-	18.1	-	13.9	ns
		DIR to nB	-	25.8	-	23.7	-	15.5	-	13.1	-	11.5	ns
OFF-state to LOW propagation delay	t_{PZL}	DIR to nA	-	37.5	-	32.5	-	20.1	-	17.8	-	14.3	ns
		DIR to nB	-	26.1	-	23.0	-	17.0	-	14.8	-	13.8	ns

$V_{CC(A)}$=3.0V to 3.6V												
LOW to HIGH propagation delay	t_{PLH}	nA to nB	-	18.9	-	17.0	-	8.7	-	6.2	-	4.9	ns
		nB to nA	-	12.9	-	8.0	-	7.0	-	6.2	-	6.0	ns
HIGH to LOW propagation delay	t_{PHL}	nA to nB	-	17.1	-	13.8	-	7.7	-	5.5	-	4.8	ns
		nB to nA	-	12.1	-	7.9	-	6.2	-	5.5	-	5.0	ns
HIGH to OFF-state propagation delay	t_{PHZ}	DIR to nA	-	8.0	-	8.0	-	8.0	-	8.0	-	8.0	ns
		DIR to nB	-	19.9	-	18.3	-	11.4	-	9.6	-	7.5	ns
LOW to OFF-state propagation delay	t_{PLZ}	DIR to nA	-	6.4	-	6.4	-	6.4	-	6.4	-	6.4	ns
		DIR to nB	-	15.2	-	14.0	-	8.8	-	8.1	-	7.5	ns
OFF-state to HIGH propagation delay	t_{PZH}	DIR to nA	-	27.5	-	21.3	-	15.2	-	13.9	-	11.0	ns
		DIR to nB	-	24.8	-	22.8	-	14.6	-	12.0	-	10.8	ns
OFF-state to LOW propagation delay	t_{PZL}	DIR to nA	-	31.3	-	25.6	-	16.8	-	14.6	-	11.6	ns
		DIR to nB	-	25.0	-	21.7	-	15.5	-	13.3	-	12.2	ns
$V_{CC(A)}$=4.5V to 5.5V												
LOW to HIGH propagation delay	t_{PLH}	nA to nB	-	18.1	-	16.5	-	8.5	-	6.2	-	4.3	ns
		nB to nA	-	11.4	-	7.3	-	5.5	-	5.0	-	4.3	ns
HIGH to LOW propagation delay	t_{PHL}	nA to nB	-	16.5	-	13.3	-	6.9	-	5.0	-	4.0	ns
		nB to nA	-	11.4	-	7.1	-	5.1	-	4.4	-	4.0	ns
HIGH to OFF-state propagation delay	t_{PHZ}	DIR to nA	-	6.0	-	6.0	-	6.0	-	6.0	-	6.0	ns
		DIR to nB	-	18.6	-	17.5	-	10.5	-	8.8	-	7.2	ns
LOW to OFF-state propagation delay	t_{PLZ}	DIR to nA	-	5.8	-	5.8	-	5.8	-	5.8	-	5.8	ns
		DIR to nB	-	14.3	-	13.0	-	8.2	-	7.8	-	7.2	ns
OFF-state to HIGH propagation delay	t_{PZH}	DIR to nA	-	25.8	-	20.6	-	13.2	-	12.0	-	9.1	ns
		DIR to nB	-	22.0	-	20.5	-	12.1	-	10.0	-	8.1	ns
OFF-state to LOW propagation delay	t_{PZL}	DIR to nA	-	30.5	-	25.6	-	15.5	-	12.8	-	10.2	ns
		DIR to nB	-	22.5	-	19.5	-	12.4	-	10.6	-	9.8	ns

4、Testing Circuit

4.1、AC Testing Circuit

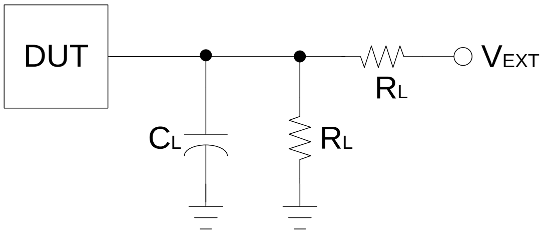


Figure 3. AC Testing Circuit

C_L includes probe and jig capacitance.

R_L=Load resistance.

Supply voltage	Load		V_{EXT}		
$V_{CC(A)}$,$V_{CC(B)}$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[1]
1.2V to 5.5V	15pF	2kΩ	open	GND	$2V_{CCO}$

Note:

[1] V_{CCO} is the supply voltage associated with the output port.

4.2、Test Condition

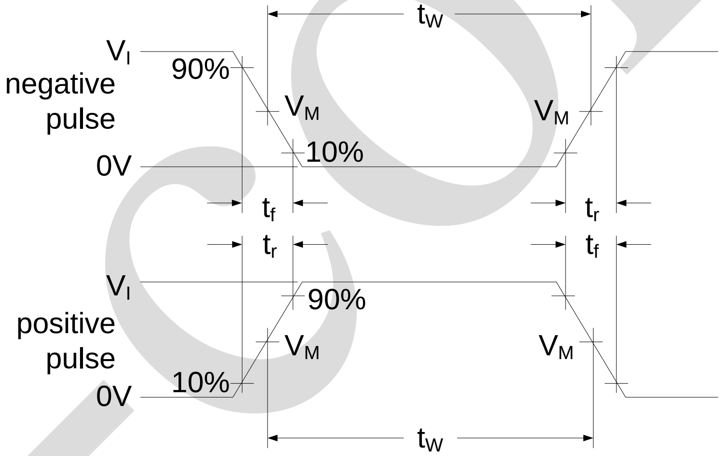


Figure 4. Test Condition

Supply voltage	Input	
$V_{CC(A)}$,$V_{CC(B)}$	V_I[1]	$t_r = t_f$
1.2V to 5.5V	V_{CCI}	≤ 3ns

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

4.3、AC Testing Waveforms

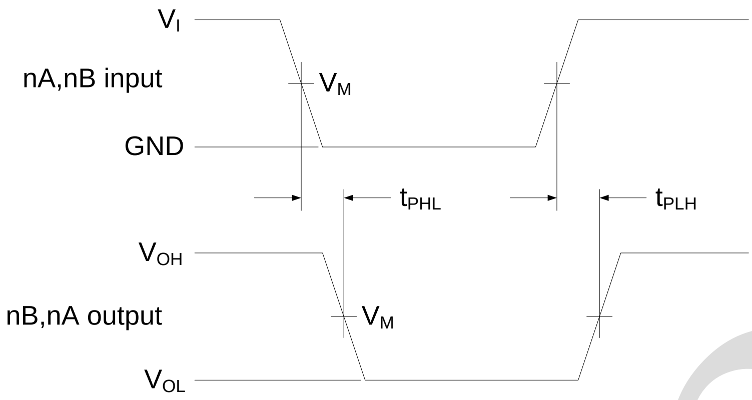


Figure 5. The data input (nA, nB) to output (nB, nA) propagation delay times

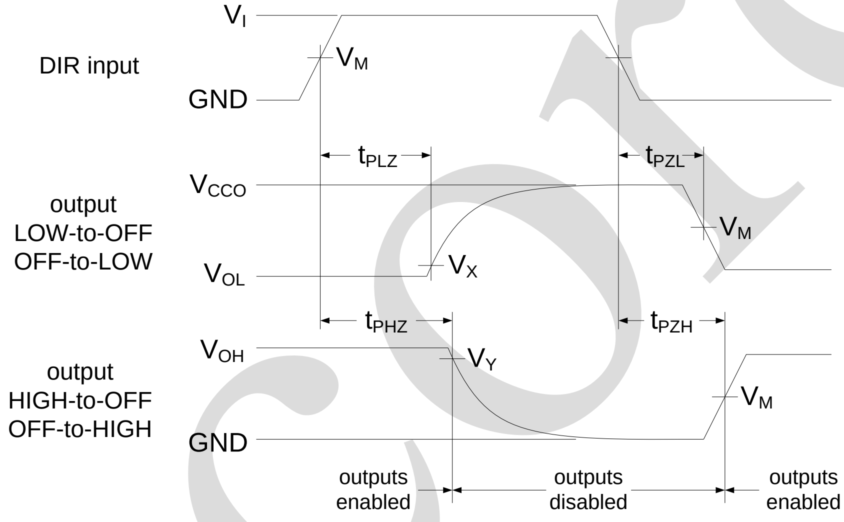


Figure 6. Enable and disable times

4.4、Measurement Points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$,$V_{CC(B)}$	**V_M**	**V_M**	**V_X**	**V_Y**
1.2V to 1.6V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.1V	V_{OH}-0.1V
1.65V to 2.7V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.15V	V_{OH}-0.15V
3.0V to 5.5V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL}+0.3V	V_{OH}-0.3V

Note:

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

5、Typical Application Circuit And Application Note

5.1、Unidirectional Logic Level-shifting Application

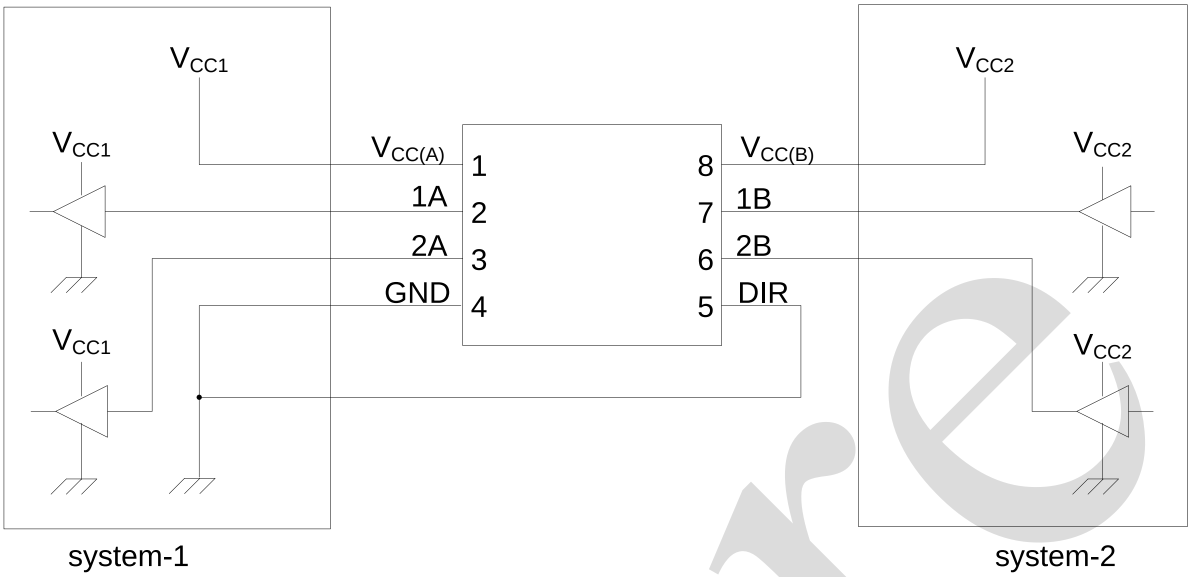


Figure 7. Unidirectional logic level-shifting application

5.2、Bidirectional Logic Level-shifting Application

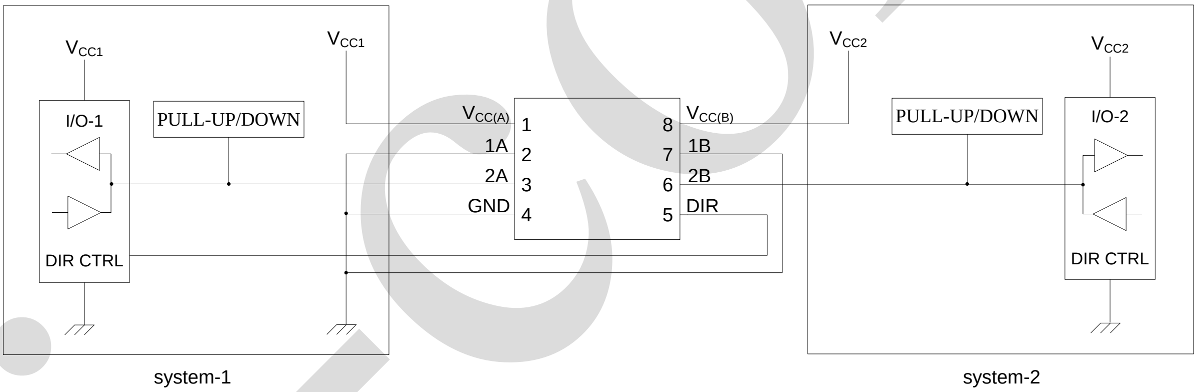
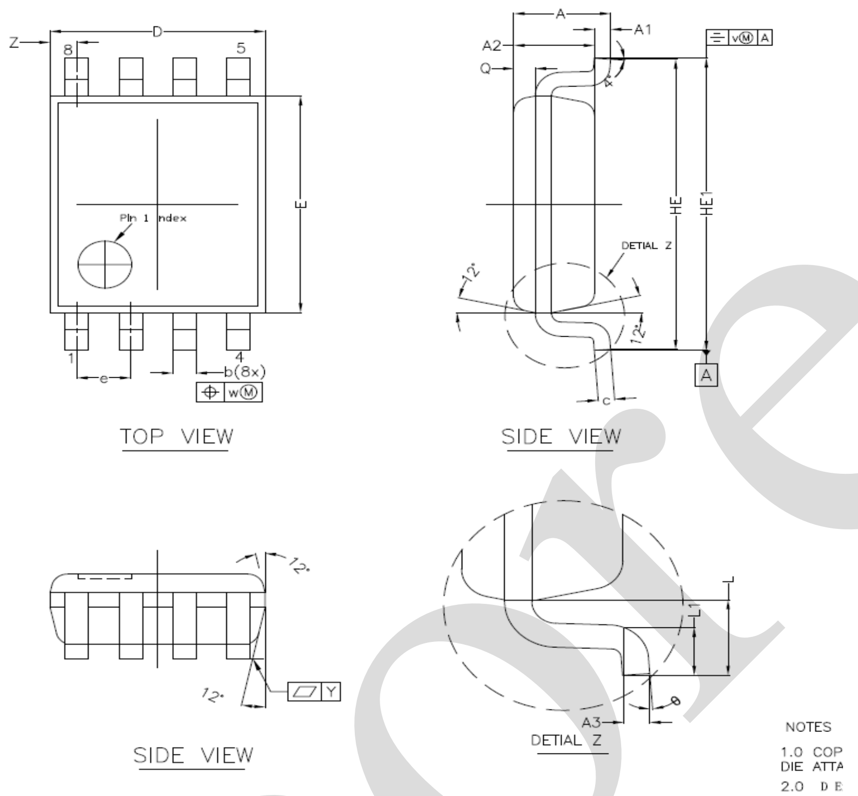


Figure 8. Bidirectional logic level-shifting application

6、Package Information

6.1、VSSOP8



Symbol	Dimensions (mm)	
	Min.	**Max.**
A	-	1.00
A1	0.00	0.15
A2	0.60	0.85
A3	0.12	
Q	0.19	0.21
b	0.17	0.27
c	0.08	0.23
D	1.90	2.10
E	2.20	2.40
HE	3.00	3.20
HE1	3.00	3.40
e	0.50	
L	0.40	
L1	0.15	0.40
Y	0.10	
Z	0.10	0.40
θ	0°	8°

7、Statements And Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We recommend you to read this chapter carefully before using this product.

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