AiP24CM01
I^2C-Compatible Serial E^2PROM

Product Specification

Specification Revision History：

Version	Date	Description
2021-01-A1	2021-01	New
2022-01-A2	2022-01	Modify Ordering Information

1、General Description

The AiP24CM01 is a 1024-Kbit I^2C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 128 K×8 bits, which is organized in 256-byte per page. AiP24CM01 provides the following devices for different application.

Features:

- Single Supply Voltage and High Speed
  Minimum operating voltage down to 1.7V
  1 MHz clock from 2.5V to 5.5V
  400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  Read current 500uA, maximum
  Write current 2.5mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 256 byte Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Page
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  Endurance: 1 Million Write Cycles
  Data Retention: 100 Years
  HBM: 6KV
  Latch up Capability: +/-200mA
- Package: DIP8, SOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP24CM01DA8.TB	DIP8	AiP24CM01	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
AiP24CM01SA8.TB	SOP8	AiP24CM01	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm

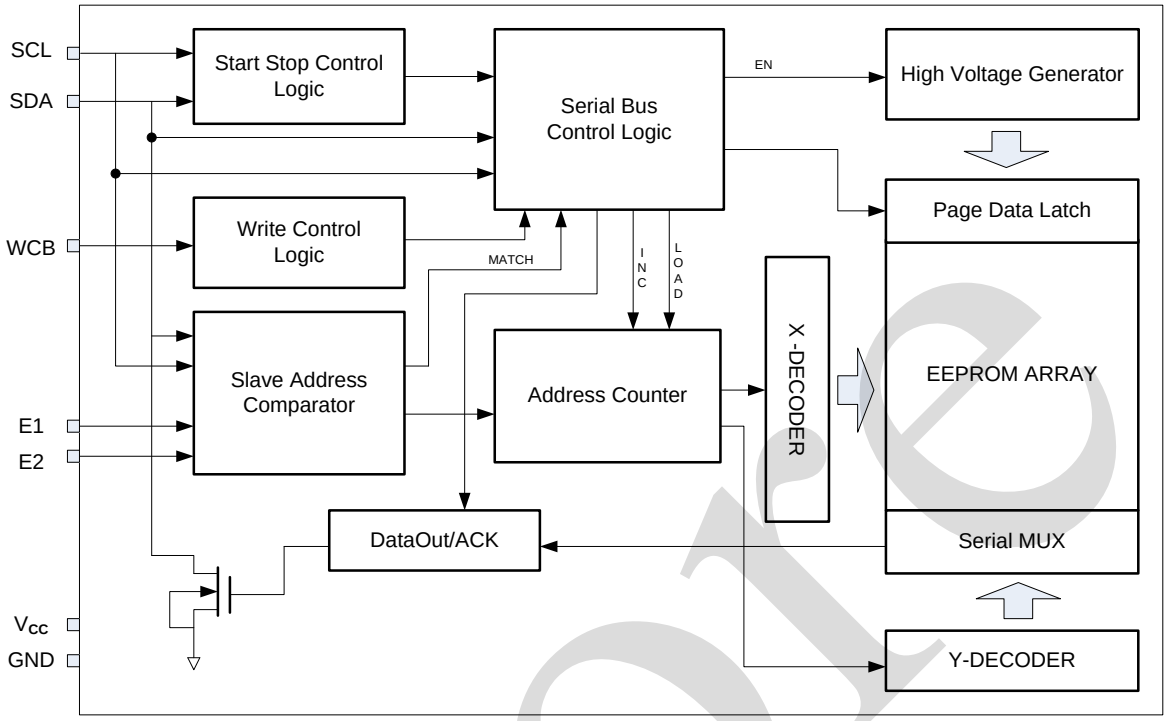
Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP24CM01SA8.TR	SOP8	AiP24CM01	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm

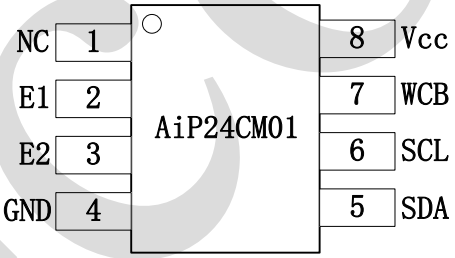
Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	NC	No Connect
2	E1	Slave Address Setting
3	E2	Slave Address Setting
4	GND	Ground
5	SDA	Serial Data Input and Serial Data Output
6	SCL	Serial Clock Input
7	WCB	Write Control, Low Enable Write
8	V_{CC}	Power

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	V_{CC}	-		6.25 (Max)	V
Voltage on Any Pin with Respect to Ground	V	-		-1.0~V_{CC}+1.0	V
DC Output Current	I	-		5.0	mA
Input/Output Capacitance (SDA) [1]	$C_{I/O}$	$V_{I/O}$=GND		8 (Max)	pF
Input Capacitance (E1,E2,WCB,SCL) [1]	C_{IN}	V_{IN}=GND		6 (Max)	pF
Operating Temperature	T_{amb}	-		-40 to 85	℃
Storage Temperature	T_{stg}	-		-65 to 150	℃
Soldering Temperature	T_L	10s	DIP	245	℃
			SOP	250	℃

Notes:

[1] Test Conditions: T_{amb}=25℃, F=1MHz, V_{CC}=5.0V.

[2] Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3.2、Electrical Characteristics

3.2.1、DC Characteristics

(T_{amb}=-40℃ to +85℃, V_{CC}=1.7V to 5.5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	1.7	-	5.5	V
Standby Current	Isb	Vcc=3.3V, T_{amb}=85℃	-	-	1.0	uA
		Vcc=5.5V, T_{amb}=85℃	-	-	3.0	uA
Supply Current	I_{CC1}	Vcc=5.5V, Read at 400Khz	-	-	0.5	mA
Supply Current	I_{CC2}	Vcc=5.5V,Write at 400Khz	-	-	2.5	mA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or GND	-	0.10	1.0	uA
Output Leakage	I_{LO}	V_{OUT}=V_{CC} or GND	-	0.05	1.0	uA
Input Low Level	V_{IL}	-	-0.6	-	0.3V_{CC}	V
Input High Level	V_{IH}	-	0.7V_{CC}	-	V_{CC}+0.5	V
Output Low Level	V_{OL1}	V_{CC}=1.7V (SDA) I_{OL}=1.5mA	-	-	0.2	V
Output Low Level	V_{OL2}	V_{CC}=3.0V (SDA) I_{OL}=2.1mA	-	-	0.4	V

3.2.2、AC Characteristics

(T_{amb}=-40℃ to +85℃, C_L=100pF, V_{CC}=1.7V to 5.5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}	V_{CC}=1.7V to 2.5V	-	-	400	KHz
		V_{CC}=2.5V to 5.5V	-	-	1000	KHz
Clock Pulse Width Low	t_{LOW}	V_{CC}=1.7V to 2.5V	1.3	-	-	us
		V_{CC}=2.5V to 5.5V	0.4	-	-	us
Clock Pulse Width High	t_{HIGH}	V_{CC}=1.7V to 2.5V	0.6	-	-	us
		V_{CC}=2.5V to 5.5V	0.4	-	-	us
Clock Low to Data Out Valid	t_{AA}	V_{CC}=1.7V to 2.5V	0.05	-	0.9	us
		V_{CC}=2.5V to 5.5V	0.05	-	0.55	us
Noise Suppression Time	t_I	V_{CC}=1.7V to 2.5V	-	-	0.1	us
		V_{CC}=2.5V to 5.5V	-	-	0.05	us
Time the bus must be free before a new transmission can start	t_{BUF}	V_{CC}=1.7V to 2.5V	1.3	-	-	us
		V_{CC}=2.5V to 5.5V	0.5	-	-	us
Start Hold Time	$t_{HD.STA}$	V_{CC}=1.7V to 2.5V	0.6	-	-	us
		V_{CC}=2.5V to 5.5V	0.25	-	-	us
Start Setup Time	$t_{SU.STA}$	V_{CC}=1.7V to 2.5V	0.6	-	-	us
		V_{CC}=2.5V to 5.5V	0.25	-	-	us
Data In Hold Time	$t_{HD.DAT}$	V_{CC}=1.7V to 2.5V	0	-	-	us
		V_{CC}=2.5V to 5.5V	0	-	-	us
Data In Setup Time	$t_{SU.DAT}$	V_{CC}=1.7V to 2.5V	0.1	-	-	us
		V_{CC}=2.5V to 5.5V	0.1	-	-	us
Inputs Rise Time[1]	t_R	V_{CC}=1.7V to 2.5V	-	-	0.3	us
		V_{CC}=2.5V to 5.5V	-	-	0.3	us
Inputs Fall Time[1]	t_F	V_{CC}=1.7V to 2.5V	-	-	0.3	us
		V_{CC}=2.5V to 5.5V	-	-	0.1	us
Stop Setup Time	$t_{SU.STO}$	V_{CC}=1.7V to 2.5V	0.6	-	-	us
		V_{CC}=2.5V to 5.5V	0.25	-	-	us
Data Out Hold Time	t_{DH}	V_{CC}=1.7V to 2.5V	0.05	-	-	us
		V_{CC}=2.5V to 5.5V	0.05	-	-	us
WCB pin Setup Time	$t_{SU.WCB}$	V_{CC}=1.7V to 2.5V	1.2	-	-	us
		V_{CC}=2.5V to 5.5V	0.6	-	-	us
WCB pin Hold Time	$t_{HD.WCB}$	V_{CC}=1.7V to 2.5V	1.2	-	-	us
		V_{CC}=2.5V to 5.5V	0.6	-	-	us
Write Cycle Time	t_{WR}	V_{CC}=1.7V to 2.5V	-	-	5	ms
		V_{CC}=2.5V to 5.5V	-	-	5	ms
Endurance	EDR	3.3V, Page mode	1000000	-	-	Write cycles
Data retention	DRET	-	100	-	-	Years

Notes:

[1] This parameter is ensured by characterization not 100% tested

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3k (2.5V, 5.5V), 10k (1.7V)

Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}

Input rise and fall times: ≤50ns

Input and output timing reference voltages: $0.5V_{CC}$

4、Function Description

4.1、Device Operation

4.1.1、Data Input

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 4-1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

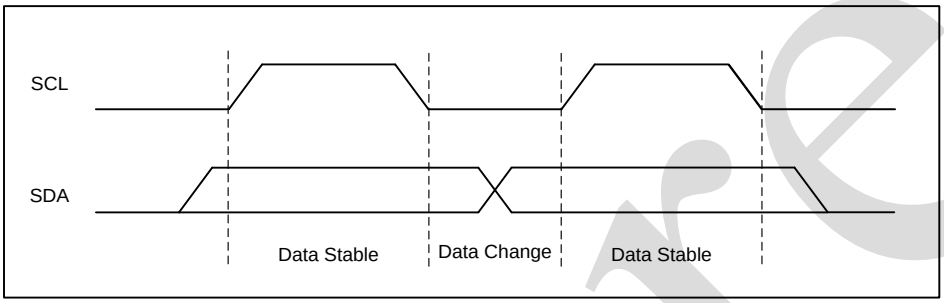


Figure 4-1

4.1.2、Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

4.1.3、Stop Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 4-2).

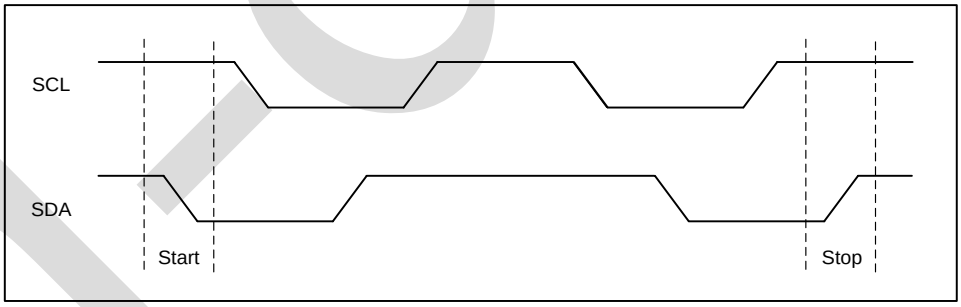


Figure 4-2

4.1.4、Acknowledge (ACK)

All addresses and data words are serially transmitted to and from the AiP24CM01 in 8-bit words. The AiP24CM01 sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

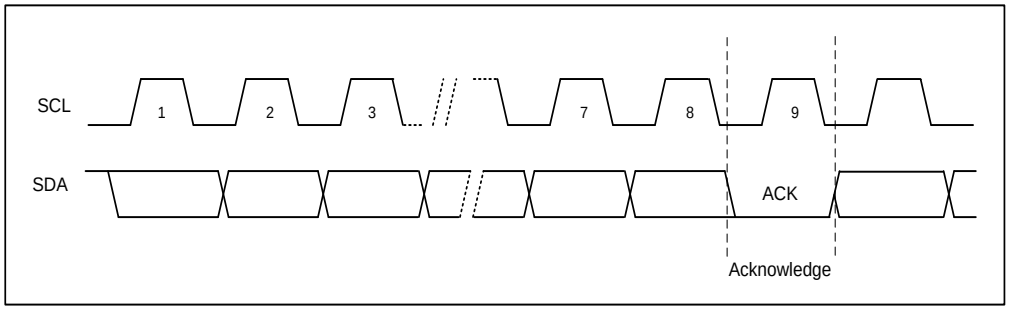


Figure 4-3

4.1.5、Standby Mode

The AiP24CM01 features a low-power standby mode which is enabled: (a) after a fresh power up, (b) after receiving a STOP bit in read mode, and (c) after completing a self-time internal programming operation

4.1.6、Soft Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps: (a) Create a start condition, (b) Clock nine cycles, and (c) create another start bit followed by stop bit condition, as shown below. The device is ready for the next communication after the above steps have been completed.

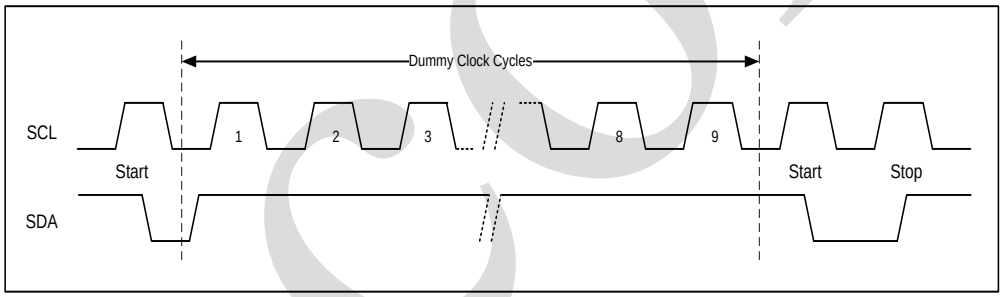


Figure 4-4

4.1.7、Bus Timing (see Figure 4-5)

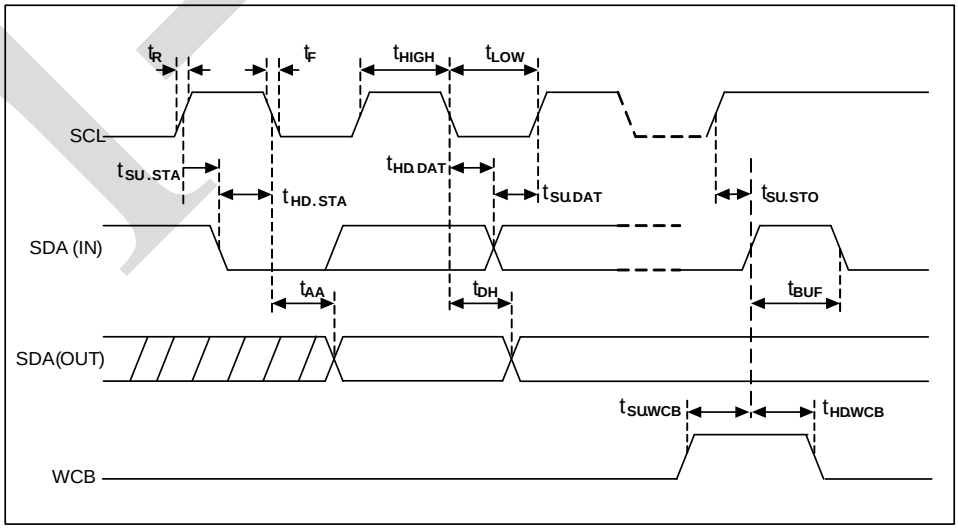


Figure 4-5

4.1.8、Write Cycle Timing (see Figure 4-6)

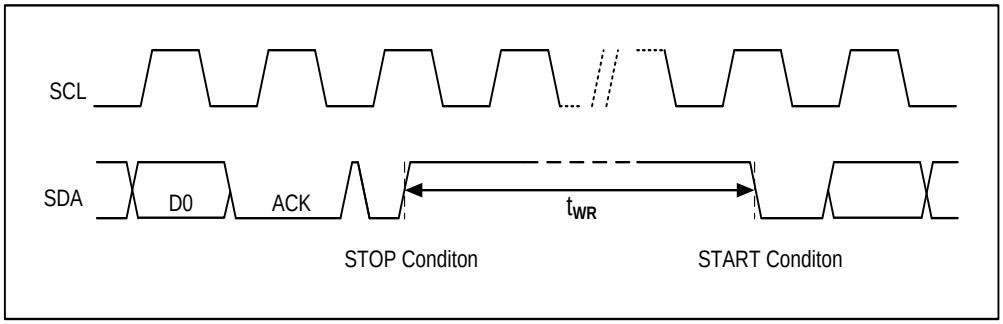


Figure 4-6

Note: [1] The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

4.2、Device Addressing

The AiP24CM01 requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure4-7). The device address word consists of a mandatory one-zero sequence for the first four most-significant bits, as shown.

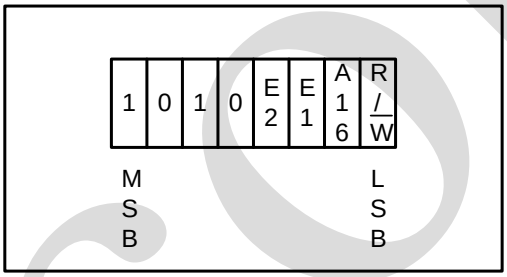


Figure4-7

The two E2 and E1 device address bits allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins.

The E2 and E1 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are floating.

The seventh bit (A16) of the device address is a memory page address bit. This memory page address bit is the most significant bit of the data word address that follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low. Upon a compare of the device address, the Chip will output a zero. If a compare is not made, the device will return to a standby state.

4.3、Data Security

AiP24CM01 has a hardware data protection scheme that allows the user to write protect the whole memory when the WCB pin is at Vcc.

4.4、Write Operations

4.4.1、Byte Write

A write operation requires 17-bit data word address following the device address word and acknowledgment. The word address field consists of the A16 bit in the device address byte, then the most significant word address (A15/A8) followed by the least significant word address (A7/A0). Upon receipt of this address, the AiP24CM01 will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the AiP24CM01 will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. And then the AiP24CM01 enters an internally timed write cycle, all inputs are disabled during this write cycle and the AiP24CM01 will not respond until the write is complete (see Figure 4-8).

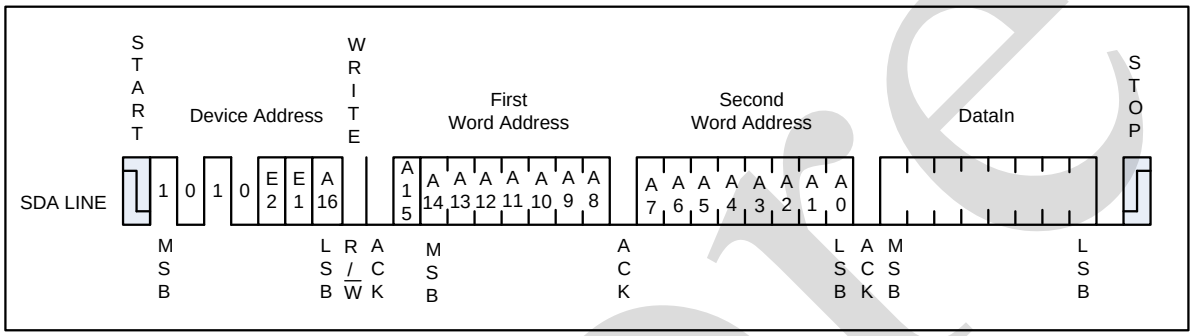
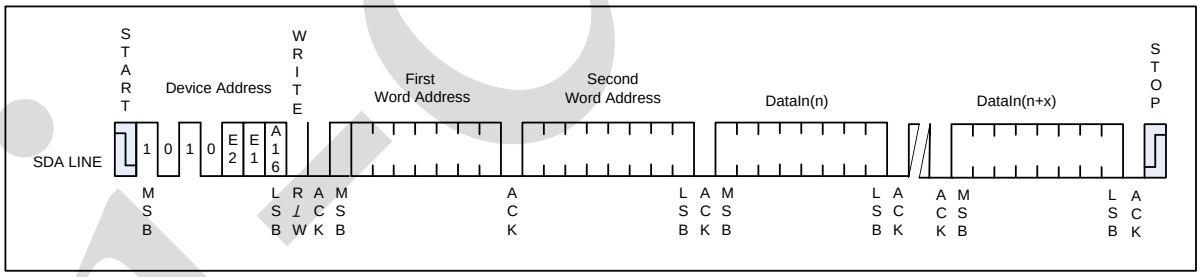


Figure 4-8

4.4.2、Page Write

A page write is initiated the same as a byte write, but the master does not send a stop condition after the first data word is clocked in. Instead, after the AiP24CM01 acknowledges receipt of the first data word, the master can transmit more data words. The AiP24CM01 will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition.



see Figure 4-9

The lower eight bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the AiP24CM01, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

4.4.3、Write Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier=1011b
- MSB address bits A16/A8 are don't care except for address bit A10 which must be '0'.

LSB address bits A7/A0 define the byte address inside the Identification page. If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

4.4.4、Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier=1011b
- Address bit A10 must be '1'; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

4.5、Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: Current Address Read; Random Address Read and Sequential Read.

4.5.1、Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the AiP24CM01, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 4-10).

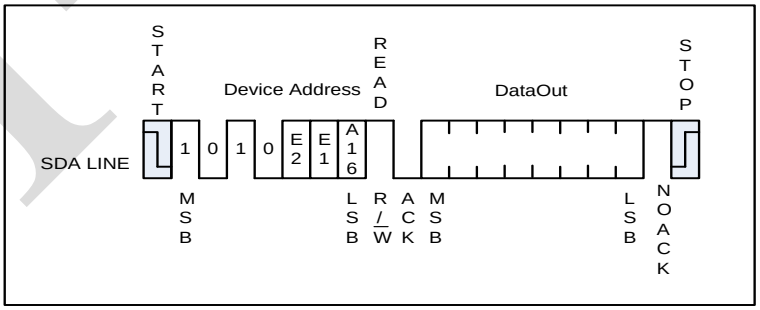


Figure 4-10

4.5.2、Random Read

A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the AiP24CM01, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The AiP24CM01 acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-11).

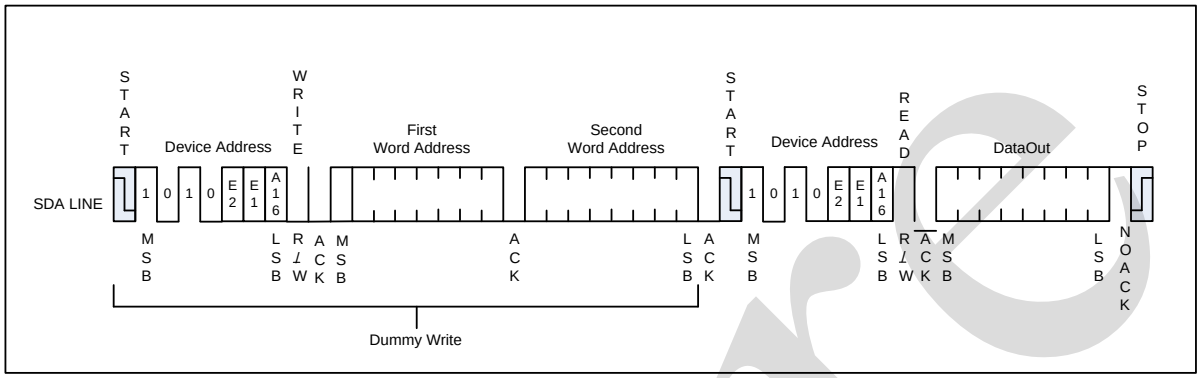


Figure 4-11

4.5.3、Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with acknowledge. As long as the AiP24CM01 receives acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a “0” but does generate a following stop condition (see Figure 4-12).

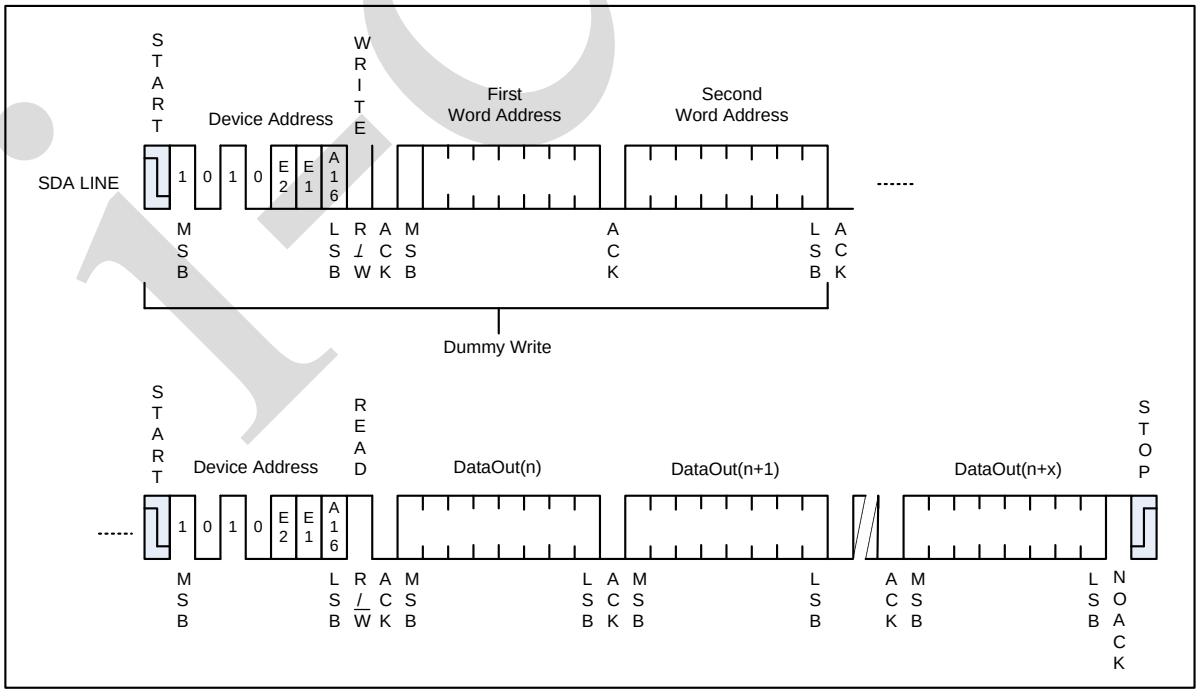


Figure 4-12

4.5.4、Read Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. The Identification Page can be read by Read Identification Page instruction which uses the same protocol and format as the Read Command (from memory array) with device type identifier defined as 1011b. The MSB address bits A16/A8 are don't care, the LSB address bits A7/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 246, as the ID page boundary is 256 bytes).

4.5.5、Read Lock Status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

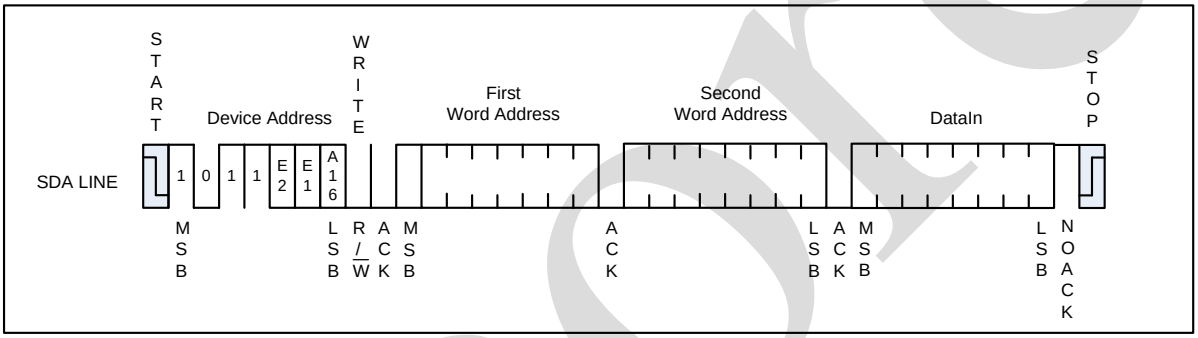
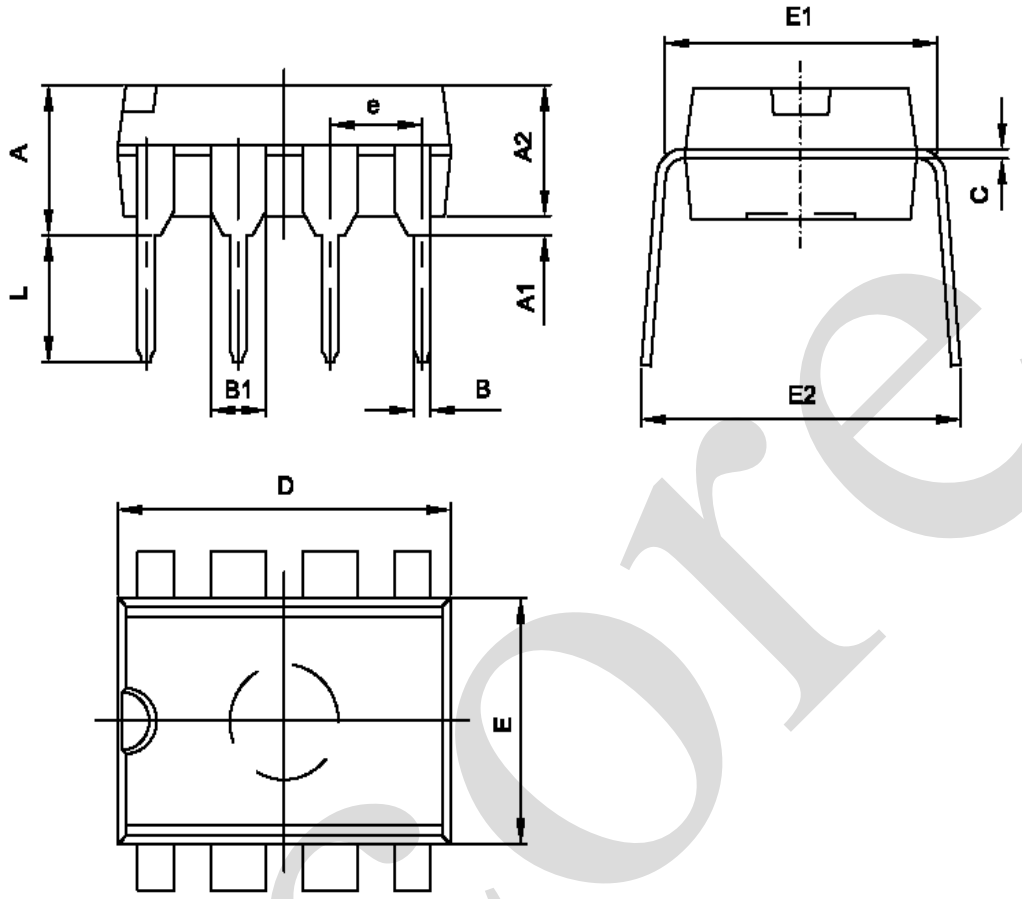


Figure 4-13

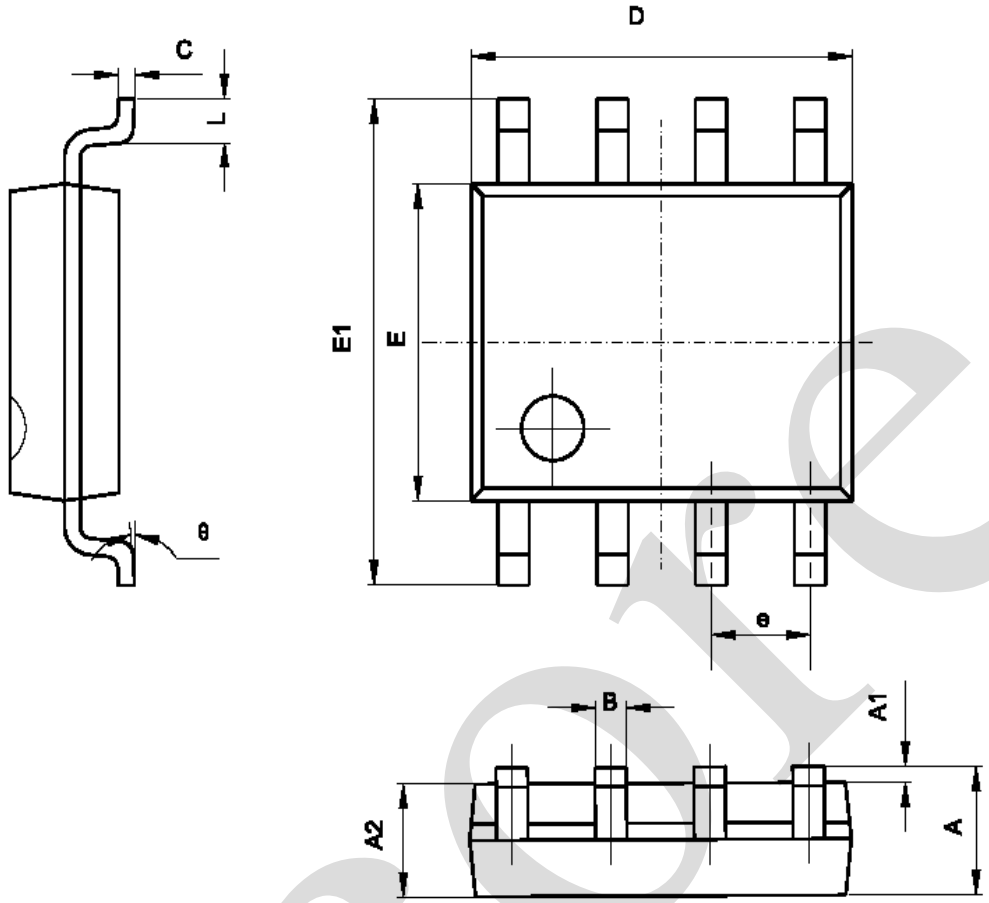
5、Package Information

5.1、DIP8



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	3.610	4.310	0.142	0.170
A1	0.510		0.020	
A2	3.100	3.600	0.122	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.200	0.360	0.008	0.014
D	9.000	9.500	0.354	0.374
E	6.100	6.600	0.240	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

5.2、SOP8



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.170	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270(TYP)		0.050(TYP)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product；

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