AiP74LVT/LVTH125
Quad Buffer/Line Driver; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2017-02-A1	2017-02	New
2023-04-B1	2023-04	Update the template

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1、General Description

The AiP74LVT/LVTH125 device combines low static and dynamic power dissipation with high speed and high output drive. This device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$ and $4\overline{OE}$), each controlling one of the 3-state outputs.

Features:

- Quad bus interface
- 3-state buffers
- Output capability: +64mA and -32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- No bus current loading when output is tied to 5V bus
- Specified from -40℃ to +125℃
- Packaging information:SOP14/TSSOP14

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVT125SA14.TB	SOP14	74LVT125	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74LVTH125SA14.TB	SOP14	74LVTH125	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
AiP74LVT125TA14.TB	TSSOP14	74LVT125	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm
AiP74LVTH125TA14.TB	TSSOP14	74LVTH125	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVT125SA14.TR	SOP14	74LVT125	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing:1.27mm
AiP74LVTH125SA14.TR	SOP14	74LVTH125	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing:1.27mm
AiP74LVT125TA14.TR	TSSOP14	74LVT125	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
AiP74LVTH125TA14.TR	TSSOP14	74LVTH125	5000PCS/reel	10000PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

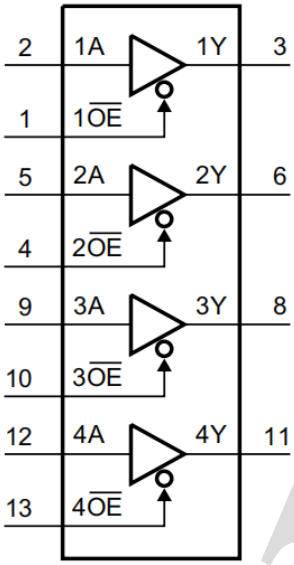


Figure 1. Logic symbol

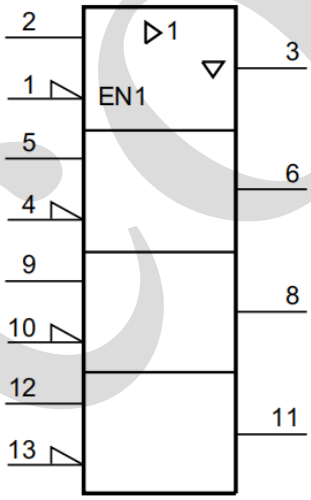


Figure 2. IEC logic symbol

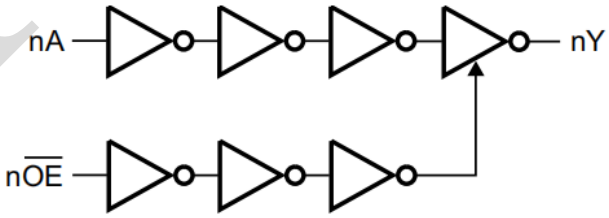
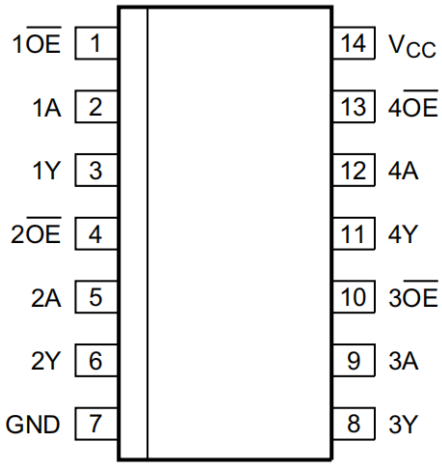


Figure 3. Logic diagram (one buffer)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1$\overline{OE}$	1 output enable input (active LOW)
2	1A	1 data input
3	1Y	1 data output
4	2$\overline{OE}$	2 output enable input (active LOW)
5	2A	2 data input
6	2Y	2 data output
7	GND	ground (0V)
8	3Y	3 data output
9	3A	3 data input
10	3$\overline{OE}$	3 output enable input (active LOW)
11	4Y	4 data output
12	4A	4 data input
13	4$\overline{OE}$	4 output enable input (active LOW)
14	V_{CC}	supply voltage

2.4、Function Table

Control	Input	Output
n$\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	X	Z

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+6.5	V
input voltage	V_I	-[1]	-0.5	+6.5	V
output voltage	V_O	output in OFF-state or HIGH-state[1]	-0.5	+6.5	V
input clamping current	I_{IK}	V_I<0V	-	-50	mA
output clamping current	I_{OK}	V_O<0V	-	-50	mA
output current	I_O	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-[2]	-	150	℃
Soldering Temperature	T_L	10s	260		℃

Note:

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.7	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
HIGH-level input voltage	V_{IH}	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	-	-	-	0.8	V
HIGH-level output current	I_{OH}	-	-	-	-32	mA
LOW-level output current	I_{OL}	none	-	-	32	mA
		current duty cycle≤50%;f≥1kHz	-	-	64	mA
input transition rise and fall rate	Δt/ΔV	-	0	-	10	ns/V
ambient temperature	T_{amb}	in free air	-40	-	+125	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
input clamping voltage	V_{IK}	I_{IK}=-18mA;V_{CC}=2.7V		-	-0.9	-1.2	V
HIGH-level output voltage	V_{OH}	I_{OH} =-100uA; V_{CC} =2.7V to 3.6V		V_{CC}-0.2	V_{CC}-0.1	-	V
		I_{OH}=-8mA; V_{CC}=2.7V		2.4	2.5	-	V
		I_{OH}=-32mA; V_{CC}=3.0V		2.0	2.2	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V	I_{OL}=100uA	-	0.1	0.2	V
			I_{OL}=24mA	-	0.3	0.5	V
		V_{CC}=3.0V	I_{OL}=16mA	-	0.25	0.4	V
			I_{OL}=32mA	-	0.3	0.5	V
			I_{OL}=64mA	-	0.4	0.55	V
input leakage current	I_I	all input pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		data pins[2]	V_{CC}=3.6V; V_I= V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-	-	-5	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
bus hold LOW current	I_{BHL}	V_{CC}=3V; V_I=0.8V[3]		75	150	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3V; V_I=2.0V		-	-150	-75	uA
bus hold LOW overdrive current	I_{BHLO}	V_{CC}=3.6V;V_I=0V to 3.6V		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=3.6V;V_I=0V to 3.6V		-	-	-500	uA
output leakage current	I_{LO}	output in HIGH-state when V_O>V_{CC}; V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; n$\overline{OE}$ = don't care[4]		-	-	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	output HIGH: V_O=3.0V	-	-	5	uA
			output LOW: V_O=0.5V	-	-	-5	uA

supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	output HIGH	-	-	0.19	mA
			output LOW	-	-	0.19	mA
			outputs disabled[5]	-	-	0.19	mA
additional supply current	ΔI_{CC}	per input pin;V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V and other inputs at V_{CC} or GND[6]		-	-	0.2	mA
input capacitance	C_I	V_I=0V or 3.0V		-	4	-	pF
output capacitance	C_O	outputs disabled; V_O=0V or 3.0V		-	8	-	pF

Note:

[1] Typical values are measured at V_{CC}=3.3V and at T_{amb}=25℃.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.0V to 3.6V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
input clamping voltage	V_{IK}	I_{IK}=-18mA;V_{CC}=2.7V		-	-	-	V
HIGH-level output voltage	V_{OH}	I_{OH}=-100uA; V_{CC}=2.7V to 3.6V		V_{CC}-0.2	-	-	V
		I_{OH}=-8mA; V_{CC}=2.7V		2.4	-	-	V
		I_{OH}=-32mA; V_{CC}=3.0V		2.0	-	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V	I_{OL}=100uA	-	-	0.2	V
			I_{OL}=24mA	-	-	0.5	V
		V_{CC}=3.0V	I_{OL}=16mA	-	-	0.4	V
			I_{OL}=32mA	-	-	0.5	V
			I_{OL}=64mA	-	-	0.55	V
input leakage current	I_I	all input pins	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
		data pins[2]	V_{CC}=3.6V; V_I= V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-	-	-5	uA

power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
bus hold LOW current	I_{BHL}	V_{CC}=3V; V_I=0.8V[3]		75	-	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3V; V_I=2.0V		-	-	-75	uA
bus hold LOW overdrive current	I_{BHLO}	V_{CC}=3.6V;V_I=0V to 3.6V		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	V_{CC}=3.6V;V_I=0V to 3.6V		-	-	-500	uA
output leakage current	I_{LO}	output in HIGH-state when V_O>V_{CC}; V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$)	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; n$\overline{OE}$ = don't care[4]		-	-	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	output HIGH: V_O=3.0V	-	-	5	uA
			output LOW: V_O=0.5V	-	-	-5	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	output HIGH	-	-	0.19	mA
			output LOW	-	-	0.19	mA
			outputs disabled[5]	-	-	0.19	mA
additional supply current	ΔI_{CC}	per input pin;V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V and other inputs at V_{CC} or GND[6]		-	-	0.2	mA

Note:

[1] Typical values are measured at V_{CC}=3.3V and at T_{amb}=25℃.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.0V to 3.6V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	nAn to nY; see Figure 5	V_{CC}=2.7V	-	-	6.3	ns
			V_{CC}=3.0V to 3.6V	1.0	3.8	5.6	ns
HIGH to LOW propagation delay	t_{PHL}	nAn to nY; see Figure 5	V_{CC}=2.7V	-	-	6.9	ns
			V_{CC}=3.0V to 3.6V	1.0	4.1	5.5	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	8.4	ns
			V_{CC}=3.0V to 3.6V	1.0	4.8	6.6	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	9.1	ns
			V_{CC}=3.0V to 3.6V	1.1	4.8	6.6	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	8.0	ns
			V_{CC}=3.0V to 3.6V	1.8	5.2	7.1	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	5.6	ns
			V_{CC}=3.0V to 3.6V	1.3	3.6	6.3	ns

Note:

[1] Typical values are measured at V_{CC}=3.3V and T_{amb}=25℃.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

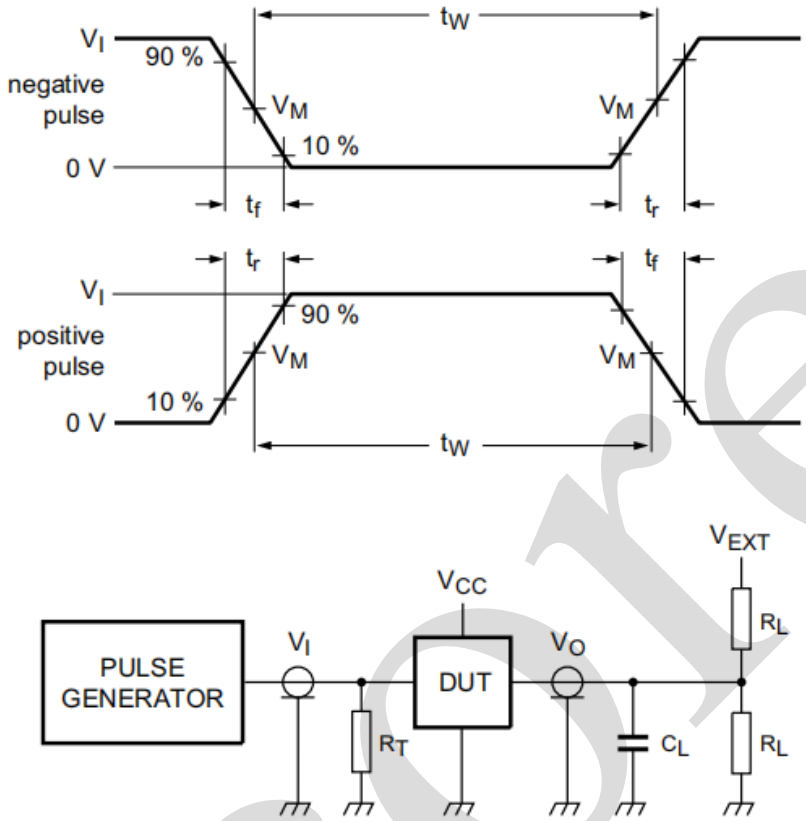
Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
LOW to HIGH propagation delay	t_{PLH}	nAn to nY; see Figure 5	V_{CC}=2.7V	-	-	7.6	ns
			V_{CC}=3.0V to 3.6V	-	-	6.7	ns
HIGH to LOW propagation delay	t_{PHL}	nAn to nY; see Figure 5	V_{CC}=2.7V	-	-	8.3	ns
			V_{CC}=3.0V to 3.6V	-	-	6.6	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	10.1	ns
			V_{CC}=3.0V to 3.6V	-	-	7.8	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	10.9	ns
			V_{CC}=3.0V to 3.6V	-	-	7.8	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	9.5	ns
			V_{CC}=3.0V to 3.6V	-	-	8.5	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nY; see Figure 6	V_{CC}=2.7V	-	-	6.7	ns
			V_{CC}=3.0V to 3.6V	-	-	7.6	ns

Note:

[1] Typical values are measured at V_{CC}=3.3V and T_{amb}=25℃.

4、Testing Circuit

4.1、AC Testing Circuit



Definitions test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

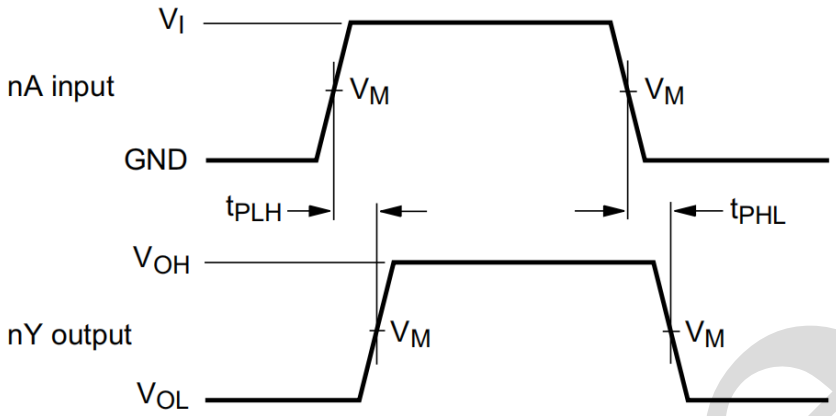
V_{EXT}=External voltage for measuring switching times.

Figure 4. Test circuit for measuring switching times

4.2、Test Data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r , t_f	C_L	R_L	t_{PHZ} , t_{PZH}	t_{PLZ} , t_{PZL}	t_{PLH} , t_{PHL}
2.7V	≤10MHz	500ns	≤2.5ns	50pF	500Ω	GND	6V	open

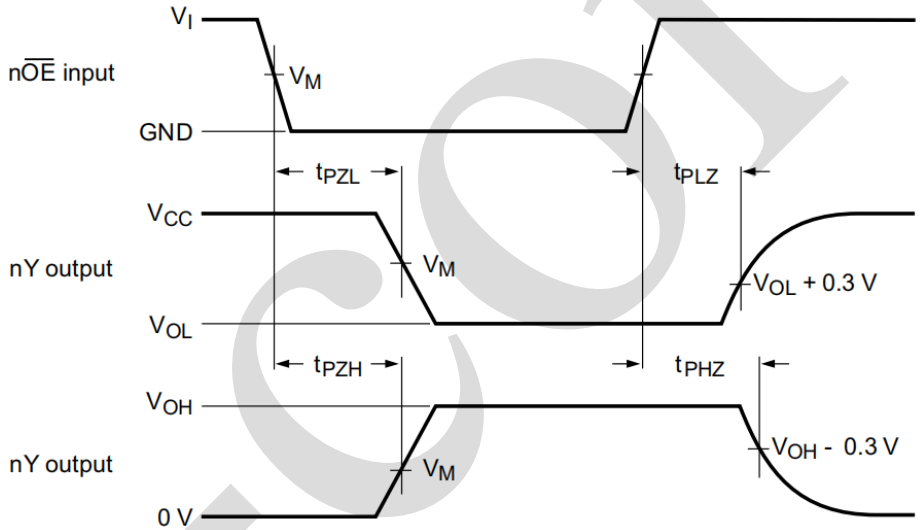
4.3、AC Testing Waveforms



V_M=1.5V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Propagation delay input (nA) to output (nY)



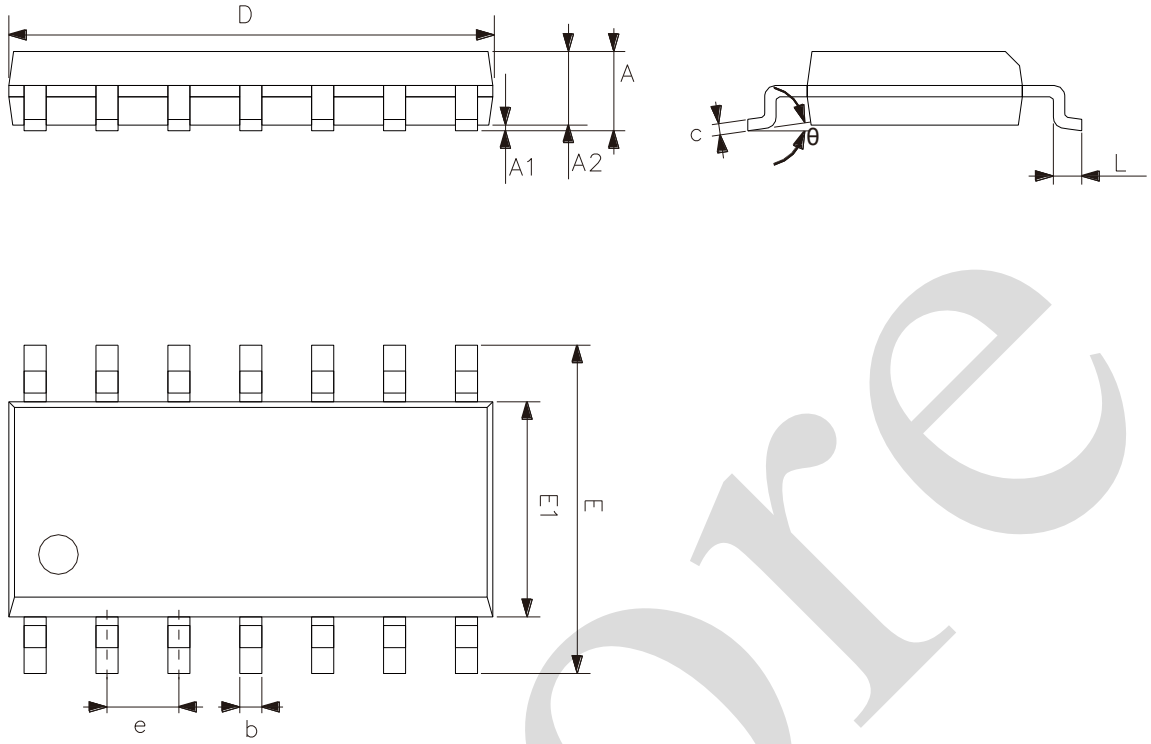
V_M=1.5V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. Enable and disable times of 3-state outputs

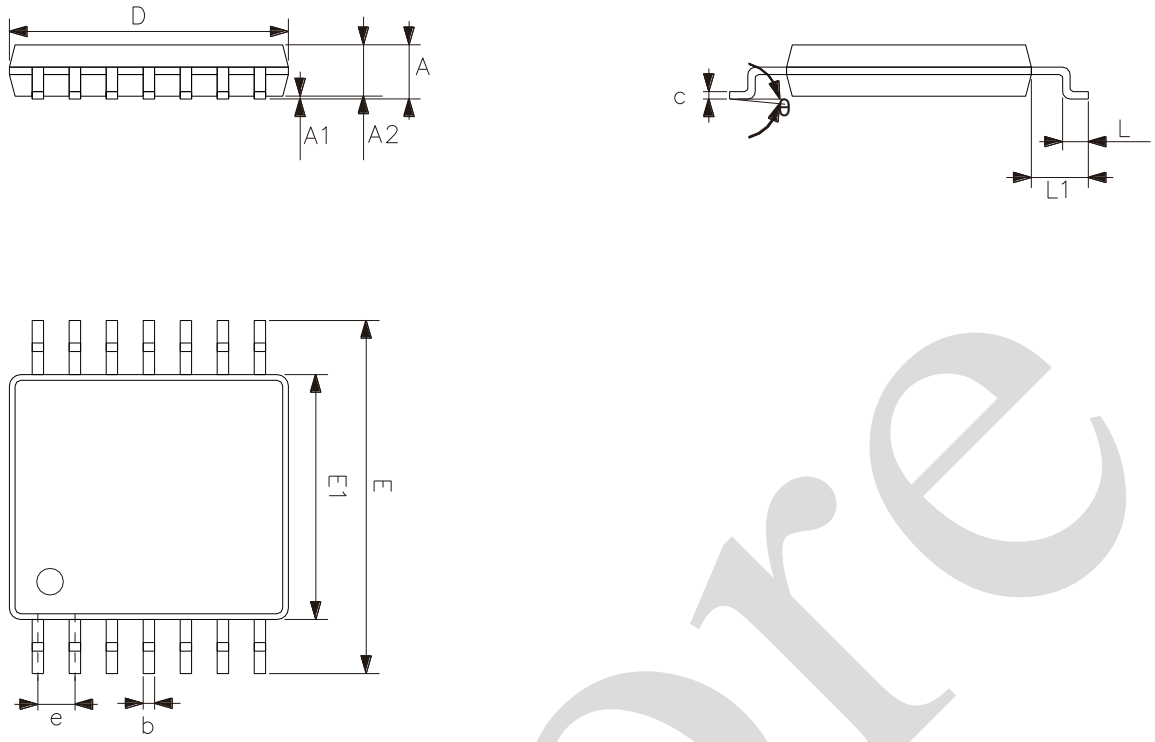
5、Package Information

5.1、SOP14



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.50	1.75
A1	0.05	0.25
A2	1.30	-
b	0.33	0.50
c	0.19	0.25
D	8.43	8.76
E	5.80	6.25
E1	3.75	4.00
e	1.27	
L	0.40	0.89
θ	0°	8°

5.2、TSSOP14



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0 °	8 °

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer' s third party users. I-Core does not accept any liability.

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