# AiP74LVT/LVTH16245
# 16-bit Bus Transceiver; 3-state

# Product Specification

**Specification Revision History:**

| Version | Date | Description |
|---|---|---|
| 2017-12-A1 | 2017-12 | New |
| 2023-04-B1 | 2023-04 | Update the template |
| | | |
| | | |

# Contents

## 1、General Description

The AiP74LVT16245; AiP74LVTH16245 is a high-performance BiCMOS product designed for $V_{CC}$ operation at 3.3V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input ($n\overline{OE}$) for easy cascading and a direction input (nDIR) for direction control.

**Features:**

- 16-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64mA and -32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5V bus
- Specified from -40℃ to +125℃
- Packaging information: TSSOP48

**Ordering Information:**

**Tube packing specifications:**

| Part number | Packaging form | Marking code | Tube quantity | Boxed tube quantity | Boxed quantity | Notes |
|---|---|---|---|---|---|---|
| AiP74LVT16245 TA48.TB | TSSOP48 | 74LVT16245 | 38 PCS/tube | 100 tube/box | 3800 PCS/box | Dimensions of plastic enclosure: 12.5mm×6.1mm Pinspacing: 0.5mm |
| AiP74LVTH16245 TA48.TB | TSSOP48 | 74LVTH16245 | 38 PCS/tube | 100 tube/box | 3800 PCS/box | Dimensions of plastic enclosure: 12.5mm×6.1mm Pinspacing: 0.5mm |

**Reel packing specifications:**

| Part number | Packaging form | Marking code | Reel quantity | Boxed reel quantity | Notes |
|---|---|---|---|---|---|
| AiP74LVT16245 TA48.TR | TSSOP48 | 74LVT16245 | 2000 PCS/reel | 2000 PCS/box | Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm |
| AiP74LVTH16245 TA48.TR | TSSOP48 | 74LVTH16245 | 2000 PCS/reel | 2000 PCS/box | Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm |

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

## 2、Block Diagram And Pin Description

### 2.1、Block Diagram

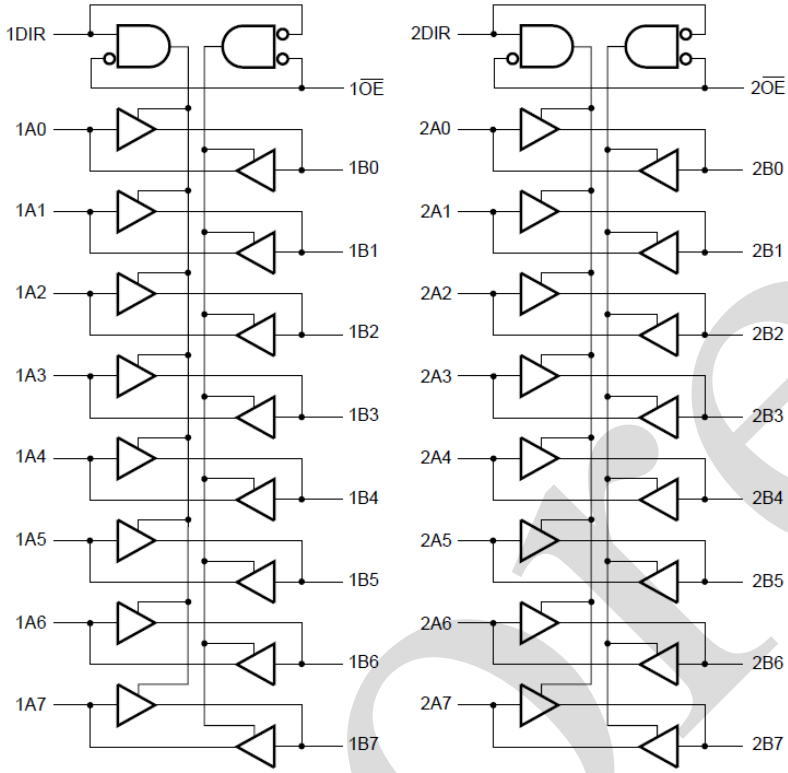



Figure 1. Logic symbol

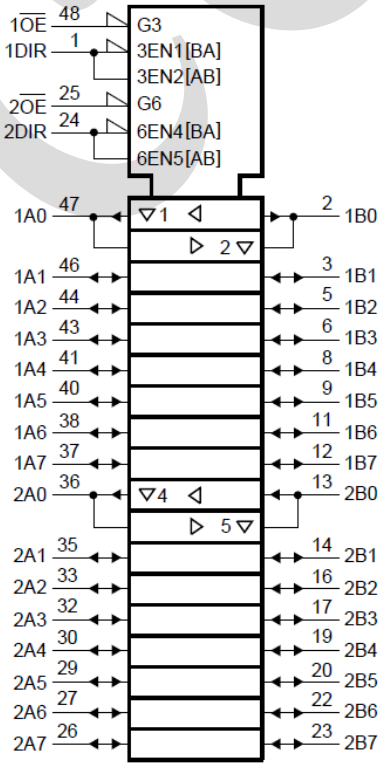
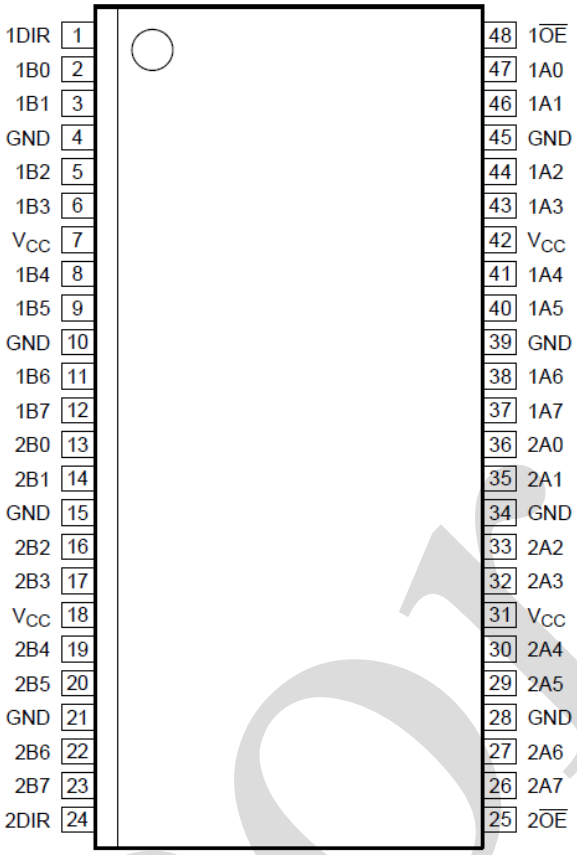



Figure 2. IEC logic symbol

## 2.2、Pin Configurations




## 2.3、Pin Description

| Pin No. | Pin Name | Description |
|---|---|---|
| 1,24 | 1DIR,2DIR | direction control inputs |
| 2,3,5,6,8,9,11,12 | 1B0,1B1,1B2,1B3,1B4,1B5,1B6,1B7 | data inputs/outputs |
| 13,14,16,17,19,20,22,23 | 2B0,2B1,2B2,2B3,2B4,2B5,2B6,2B7 | data inputs/outputs |
| 4,10,15,21,28,34,39,45 | GND | ground (0V) |
| 7,18,31,42 | $V_{CC}$ | supply voltage |
| 48,25 | $1\overline{OE}$ ,$2\overline{OE}$ | output enable inputs (active LOW) |
| 36,35,33,32,30,29,27,26 | 2A0,2A1,2A2,2A3,2A4,2A5,2A6,2A7 | data inputs/outputs |
| 47,46,44,43,41,40,38,37 | 1A0,1A1,1A2,1A3,1A4,1A5,1A6,1A7 | data inputs/outputs |

## 2.4、Function Table

| Control | | Input/Output | |
|---|---|---|---|
| **n$\overline{OE}$** | **nDIR** | **nAn** | **nBn** |
| L | L | output nAn=nBn | input |
| L | H | input | output nBn=nAn |
| H | X | Z | Z |

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care; Z=high-impedance OFF-state.

## 3、Electrical Parameter

### 3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | -0.5 | +4.6 | V |
| input voltage | $V_I$ | -[1] | -0.5 | +7.0 | V |
| output voltage | $V_O$ | output in OFF-state or HIGH-state[1] | -0.5 | +7.0 | V |
| input clamping current | $I_{IK}$ | $V_I$<0V | -50 | - | mA |
| output clamping current | $I_{OK}$ | $V_O$<0V | -50 | - | mA |
| output current | $I_O$ | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | -64 | - | mA |
| storage temperature | $T_{stg}$ | - | -65 | +150 | ℃ |
| junction temperature | $T_j$ | -[2] | - | 150 | ℃ |
| total power dissipation | $P_{tot}$ | - | - | 500 | mW |
| Soldering temperature | $T_L$ | 10s | 260 | | ℃ |

Note:

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

### 3.2、Recommended Operating Conditions

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| supply voltage | $V_{CC}$ | - | 2.7 | - | 3.6 | V |
| input voltage | $V_I$ | - | 0 | - | 5.5 | V |
| HIGH-level input voltage | $V_{IH}$ | - | 2.0 | - | - | V |
| LOW-level input voltage | $V_{IL}$ | - | - | - | 0.8 | V |
| HIGH-level output current | $I_{OH}$ | - | -32 | - | - | mA |
| LOW-level output current | $I_{OL}$ | none | - | - | 32 | mA |
| | | current duty cycle≤50%; $f_i$ ≥1kHz | - | - | 64 | mA |
| ambient temperature | $T_{amb}$ | in free-air | -40 | - | +125 | ℃ |
| input transition rise and fall rate | Δt/ΔV | outputs enabled | - | - | 10 | ns/V |

### 3.3、Electrical Characteristics

#### 3.3.1、DC Characteristics 1

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. [1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| input clamping voltage | $V_{IK}$ | $V_{CC}$=2.7V; $I_{IK}$=-18mA | | -1.2 | -0.85 | - | V |
| HIGH-level output voltage | $V_{OH}$ | $I_{OH}$ =-100uA; $V_{CC}$ =2.7V to 3.6V | | $V_{CC}$-0.2 | $V_{CC}$ | - | V |
| | | $I_{OH}$=-8mA; $V_{CC}$=2.7V | | 2.4 | 2.5 | - | V |
| | | $I_{OH}$=-32mA; $V_{CC}$=3.0V | | 2.0 | 2.3 | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_{CC}$=2.7V | $I_{OL}$=100uA | - | 0.07 | 0.2 | V |
| | | | $I_{OL}$=24mA | - | 0.3 | 0.5 | V |
| | | $V_{CC}$=3.0V | $I_{OL}$=16mA | - | 0.25 | 0.4 | V |
| | | | $I_{OL}$=32mA | - | 0.3 | 0.5 | V |
| | | | $I_{OL}$=64mA | - | 0.4 | 0.55 | V |
| input leakage current | $I_I$ | control pins | $V_{CC}$=3.6V; $V_I$=$V_{CC}$ or GND | - | - | ±1 | uA |
| | | | $V_{CC}$=0V or 3.6V; $V_I$=5.5V | - | - | 10 | uA |
| | | Input/output data pins; $V_{CC}$=3.6V[2] | $V_I$=5.5V | - | - | 20 | uA |
| | | | $V_I$= $V_{CC}$ | - | - | 10 | uA |
| | | | $V_I$=0V | -5 | - | - | uA |
| power-off leakage current | $I_{OFF}$ | $V_{CC}$=0V; $V_I$ or $V_O$=0V to 4.5V | | - | - | ±100 | uA |
| bus hold LOW current | $I_{BHL}$ | $V_{CC}$=3V; $V_I$=0.8V | | 75 | 135 | - | uA |
| bus hold HIGH current | $I_{BHH}$ | $V_{CC}$=3V; $V_I$=2.0V | | - | -135 | -75 | uA |
| bus hold LOW overdrive current | $I_{BHLO}$ | nAn input; $V_{CC}$=0V to 3.6V; $V_{CC}$=3.6V[3] | | 500 | - | - | uA |
| bus hold HIGH overdrive current | $I_{BHHO}$ | nAn input; $V_{CC}$=0V to 3.6V; $V_{CC}$=3.6V[3] | | - | - | -500 | uA |
| output leakage current | $I_{LO}$ | output in HIGH-state when $V_O$>$V_{CC}$;$V_O$=5.5V; $V_{CC}$=3.0V | | - | - | 125 | uA |
| power-up/ power-down output current | $I_{O(pu/pd)}$ | $V_{CC}$≤1.2V; $V_O$=0.5V to $V_{CC}$; $V_I$=GND or $V_{CC}$; $\overline{nOE}$ = don't care[4] | | - | - | ±100 | uA |
| supply current | $I_{CC}$ | $V_{CC}$=3.6V; $V_I$=GND or $V_{CC}$; $I_O$=0A | output HIGH | - | - | 0.12 | mA |
| | | | output LOW | - | - | 0.12 | mA |
| | | | outputs disabled[5] | - | - | 0.12 | mA |
| additional supply current | $\Delta I_{CC}$ | per input pin; $V_{CC}$=3.0V to 3.6V; one input at $V_{CC}$-0.6V, other inputs at $V_{CC}$ or GND[6] | | - | - | 0.2 | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| input capacitance | $C_I$ | pins nDIR and n$\overline{OE}$, $V_O$=0V or 3.0V | - | 3 | - | pF |
| off-state input/output capacitance | $C_{io(off)}$ | pins nAn and nBn,outputs disabled; $V_O$=GND or $V_{CC}$ | - | 9 | - | pF |

Note:

[1] Typical values are measured at $V_{CC}$=3.3V and at $T_{amb}$=25℃.

[2] Unused pins at $V_{CC}$ or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any $V_{CC}$ between 0V and 1.2V with a transition time of up to 10ms. From $V_{CC}$=1.2V to $V_{CC}$=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for $T_{amb}$=25℃ only.

[5] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

### 3.3.2、DC Characteristics 2

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ. [1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| input clamping voltage | $V_{IK}$ | $V_{CC}$=2.7V; $I_{IK}$=-18mA | | -1.2 | - | - | V |
| HIGH-level output voltage | $V_{OH}$ | $I_{OH}$=-100uA; $V_{CC}$=2.7V to 3.6V | | $V_{CC}$-0.2 | - | - | V |
| | | $I_{OH}$=-8mA; $V_{CC}$=2.7V | | 2.4 | - | - | V |
| | | $I_{OH}$=-32mA; $V_{CC}$=3.0V | | 2.0 | - | - | V |
| LOW-level output voltage | $V_{OL}$ | $V_{CC}$=2.7V | $I_{OL}$=100uA | - | - | 0.2 | V |
| | | | $I_{OL}$=24mA | - | - | 0.5 | V |
| | | $V_{CC}$=3.0V | $I_{OL}$=16mA | - | - | 0.4 | V |
| | | | $I_{OL}$=32mA | - | - | 0.5 | V |
| | | | $I_{OL}$=64mA | - | - | 0.55 | V |
| input leakage current | $I_I$ | control pins | $V_{CC}$=3.6V; $V_I$=$V_{CC}$ or GND | - | - | ±1 | uA |
| | | | $V_{CC}$=0V or 3.6V; $V_I$=5.5V | - | - | 10 | uA |
| | | Input/output data pins; $V_{CC}$=3.6V[2] | $V_I$=5.5V | - | - | 20 | uA |
| | | | $V_I$= $V_{CC}$ | - | - | 10 | uA |
| | | | $V_I$=0V | -5 | - | - | uA |
| power-off leakage current | $I_{OFF}$ | $V_{CC}$=0V; $V_I$ or $V_O$=0V to 4.5V | | - | - | ±100 | uA |
| bus hold LOW current | $I_{BHL}$ | $V_{CC}$=3V; $V_I$=0.8V | | 75 | - | - | uA |
| bus hold HIGH current | $I_{BHH}$ | $V_{CC}$=3V; $V_I$=2.0V | | - | - | -75 | uA |
| bus hold LOW overdrive current | $I_{BHLO}$ | nAn input; $V_{CC}$=0V to 3.6V; $V_{CC}$=3.6V[3] | | 500 | - | - | uA |

| | | | | | | |
|---|---|---|---|---|---|---|
| bus hold HIGH overdrive current | $I_{BHHO}$ | nAn input; $V_{CC}$=0V to 3.6V; $V_{CC}$=3.6V[3] | - | - | -500 | uA |
| output leakage current | $I_{LO}$ | output in HIGH-state when $V_O$>$V_{CC}$;$V_O$=5.5V; $V_{CC}$=3.0V | - | - | 125 | uA |
| power-up/ power-down output current | $I_{O(pu/pd)}$ | $V_{CC}$≤1.2V; $V_O$=0.5V to $V_{CC}$; $V_I$=GND or $V_{CC}$; $n\overline{OE}$ = don't care[4] | - | - | ±100 | uA |
| supply current | $I_{CC}$ | $V_{CC}$=3.6V; $V_I$=GND or $V_{CC}$; $I_O$=0A; output HIGH | - | - | 0.12 | mA |
| | | output LOW | - | - | 0.12 | mA |
| | | outputs disabled[5] | - | - | 0.12 | mA |
| additional supply current | $\Delta I_{CC}$ | per input pin; $V_{CC}$=3.0V to 3.6V; one input at $V_{CC}$-0.6V, other inputs at $V_{CC}$ or GND[6] | - | - | 0.2 | mA |

Note:

[1] Typical values are measured at $V_{CC}$=3.3V and at $T_{amb}$=25℃.

[2] Unused pins at $V_{CC}$ or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any $V_{CC}$ between 0V and 1.2V with a transition time of up to 10ms. From $V_{CC}$=1.2V to $V_{CC}$=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for $T_{amb}$=25℃ only.

[5] $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.

### 3.3.3、AC Characteristics 1

($T_{amb}$=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| LOW to HIGH propagation delay | $t_{PLH}$ | nAn to nBn or nBn to nAn; see Figure 4 | $V_{CC}$=2.7V | - | - | 4.9 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.0 | 2.7 | 4.6 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | nAn to nBn or nBn to nAn; see Figure 4 | $V_{CC}$=2.7V | - | - | 4.9 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.0 | 2.4 | 4.6 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | $n\overline{OE}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 7.4 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.0 | 3.9 | 6.3 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | $n\overline{OE}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 7.1 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.0 | 3.9 | 5.7 | ns |
| HIGH to OFF-state propagation delay | $t_{PHZ}$ | $n\overline{OE}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 8.0 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.5 | 4.5 | 7.1 | ns |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| LOW to OFF-state propagation delay | $t_{PLZ}$ | $\overline{n\text{OE}}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 6.4 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | 1.5 | 4.2 | 6.4 | ns |

Note:

[1] Typical values are measured at $V_{CC}$=3.3V and $T_{amb}$=25℃.

### 3.3.4、AC Characteristics 2

($T_{amb}$=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

| Parameter | Symbol | Conditions | | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| LOW to HIGH propagation delay | $t_{PLH}$ | nAn to nBn or nBn to nAn; see Figure 4 | $V_{CC}$=2.7V | - | - | 5.9 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 5.6 | ns |
| HIGH to LOW propagation delay | $t_{PHL}$ | nAn to nBn or nBn to nAn; see Figure 4 | $V_{CC}$=2.7V | - | - | 5.9 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 5.6 | ns |
| OFF-state to HIGH propagation delay | $t_{PZH}$ | $\overline{n\text{OE}}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 9.0 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 7.6 | ns |
| OFF-state to LOW propagation delay | $t_{PZL}$ | $\overline{n\text{OE}}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 8.5 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 6.9 | ns |
| HIGH to OFF-state propagation delay | $t_{PHZ}$ | $\overline{n\text{OE}}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 9.5 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 8.5 | ns |
| LOW to OFF-state propagation delay | $t_{PLZ}$ | $\overline{n\text{OE}}$ to nAn or nBn; see Figure 5 | $V_{CC}$=2.7V | - | - | 7.7 | ns |
| | | | $V_{CC}$=3.0V to 3.6V | - | - | 7.7 | ns |

Note:

[1] Typical values are measured at $V_{CC}$=3.3V and $T_{amb}$=25℃.

## 4、Testing Circuit

### 4.1、AC Testing Circuit

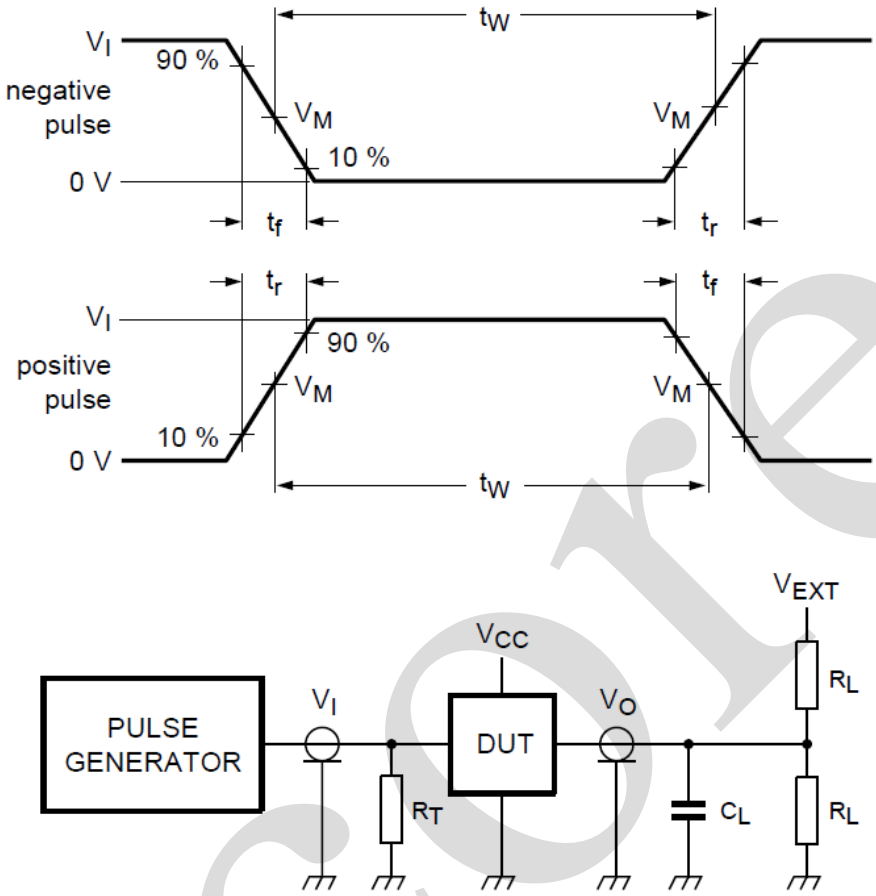



Figure 3. Test circuit for measuring switching times

Definitions test circuit:

$R_L$=Load resistance.

$C_L$=Load capacitance including jig and probe capacitance.

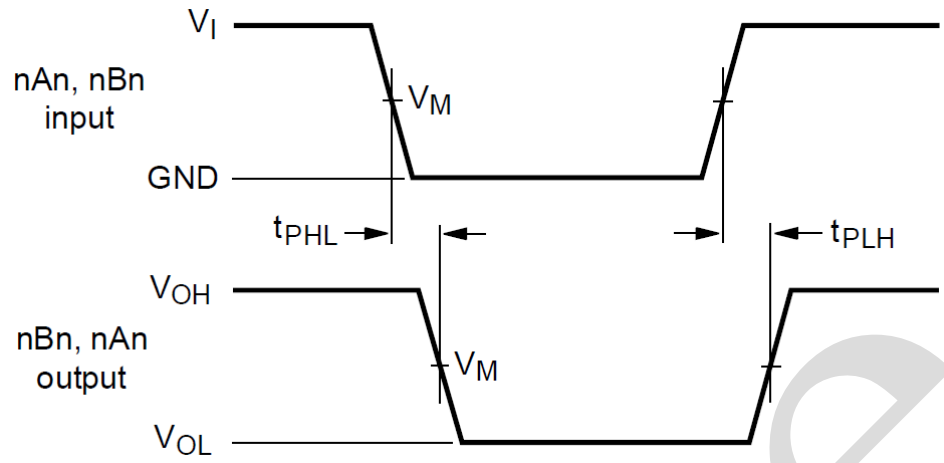
$R_T$=Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$=External voltage for measuring switching times.

### 4.2、Test Data

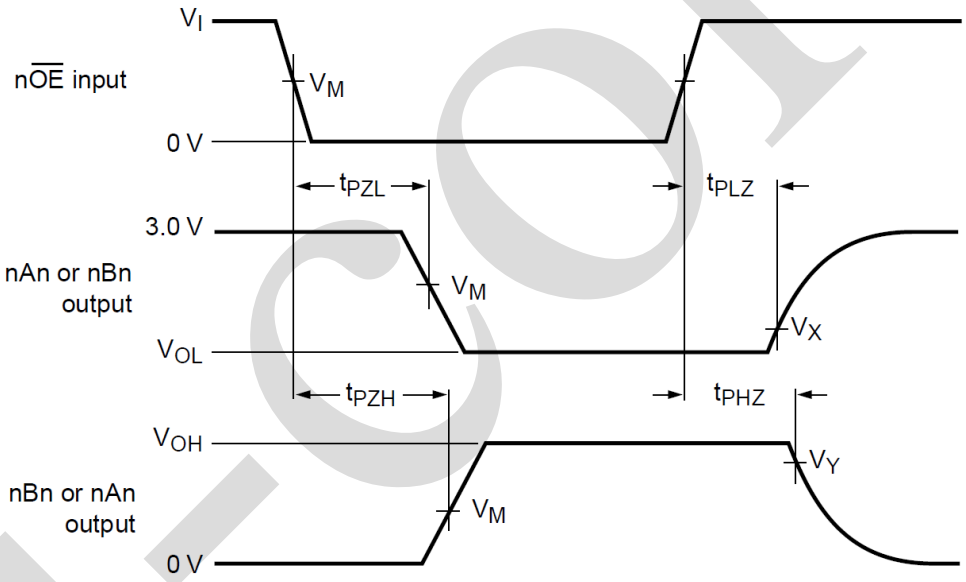
| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$ , $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$ , $t_{PZH}$ | $t_{PLZ}$ , $t_{PZL}$ | $t_{PLH}$ , $t_{PHL}$ |
| 2.7V | ≤10MHz | 500ns | ≤2.5ns | 50pF | 500Ω | GND | 6V | open |

### 4.3、AC Testing Waveforms




$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

Figure 4.Propagation delay input (nAn, nBn) to output (nBn, nAn)




$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

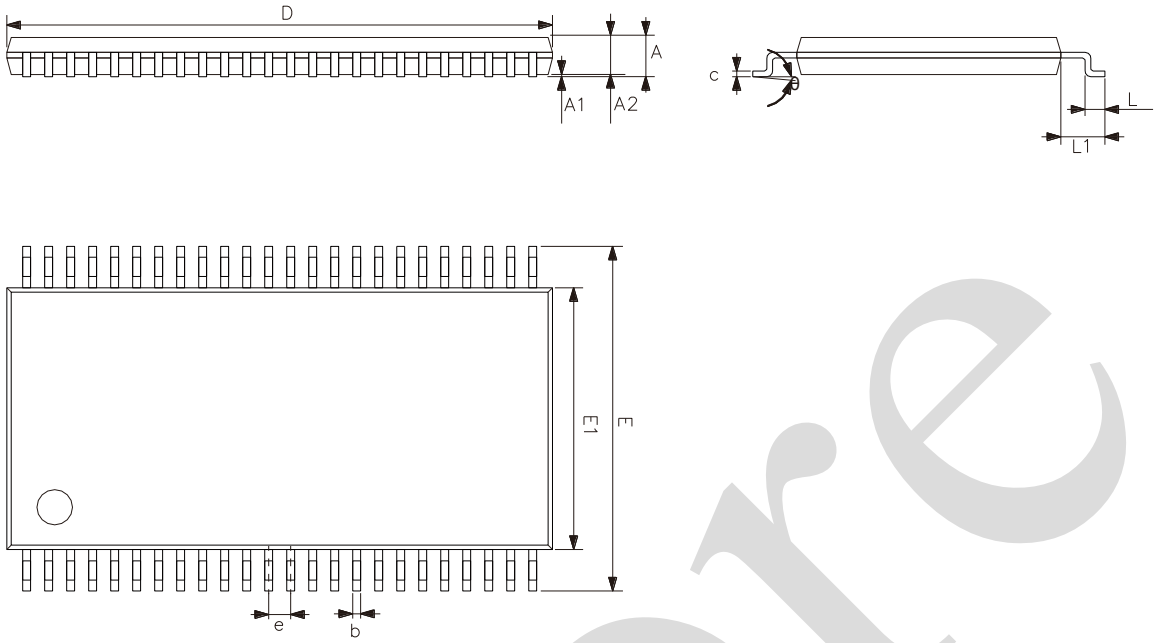
Figure 5. 3-state output enable and disable times

### 4.4、Measurement Points

| Input | Output | | |
|---|---|---|---|
| $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.5V | 1.5V | $V_{OL}$+0.3V | $V_{OH}$-0.3V |

# 5、Package Information

## 5.1、TSSOP48




| Symbol | Dimensions (mm) | |
|---|---|---|
| | Min. | Max. |
| A | - | 1.20 |
| A1 | 0.03 | 0.15 |
| A2 | 0.82 | 1.05 |
| b | 0.17 | 0.27 |
| c | 0.12 | 0.22 |
| D | 12.40 | 12.60 |
| E | 7.90 | 8.30 |
| E1 | 6.00 | 6.20 |
| e | 0.50 | |
| L | 0.35 | 0.75 |
| L1 | 1.00 | |
| θ | 0° | 8° |

## 6、Statements And Notes

### 6.1、The name and content of Hazardous substances or Elements in the product

| Part name | Hazardous substances or Elements | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Lead and lead compounds | Mercury and mercury compounds | Cadmium and cadmium compounds | Hexavalent chromium compounds | Polybrominated biphenyls | Polybrominated biphenyl ethers | Dibutyl phthalate | Butylbenzyl phthalate | Di-2-ethylhexyl phthalate | Diisobutyl phthalate |
| Lead frame | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic resin | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Chip | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| The lead | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| Plastic sheet installed | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ | ○ |
| explanation | ○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard.<br>×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements. | | | | | | | | | |

### 6.2、Notes

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