AiP74LVT/LVTH16374
16-bit D-type flip-flop; positive edge-trigger; 3-state

Product Specification

Specification Revision History:

Version	Date	Description
2017-12-A1	2017-12	New
2023-04-B1	2023-04	Update the template

Contents

1、General Description

The AiP74LVT16374; AiP74LVTH16374 are high performance BiCMOS products designed for V_{CC} operation at 3.3V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (nCP), the nQn outputs of the flip-flop take on the logic levels set up at the nDn inputs.

Features:

- 16-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64mA and -32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5V bus
- Specified from -40℃ to +125℃
- Packaging information: TSSOP48

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74LVT16374 TA48.TB	TSSOP48	74LVT16374	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plasticen closure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVTH16374 TA48.TB	TSSOP48	74LVTH16374	38 PCS/tube	100 tube/box	3800 PCS/box	Dimensions of plasticen closure: 12.5mm×6.1mm Pin spacing: 0.5mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74LVT16374 TA48.TR	TSSOP48	74LVT16374	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm
AiP74LVTH16374 TA48.TR	TSSOP48	74LVTH16374	2000 PCS/reel	2000 PCS/box	Dimensions of plastic enclosure: 12.5mm×6.1mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

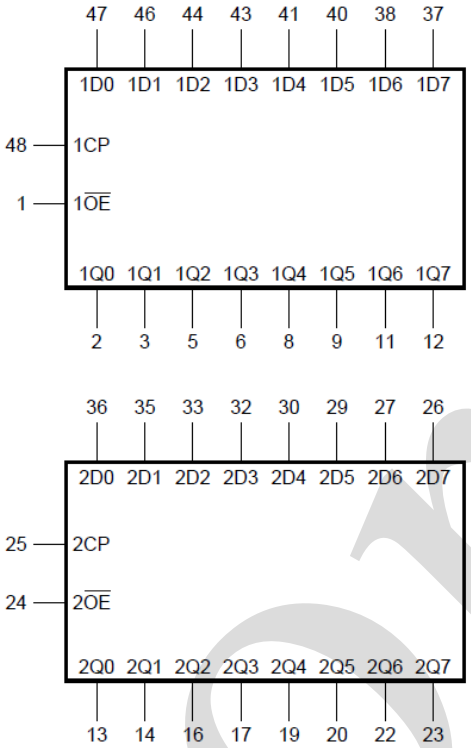


Figure 1. Logic symbol

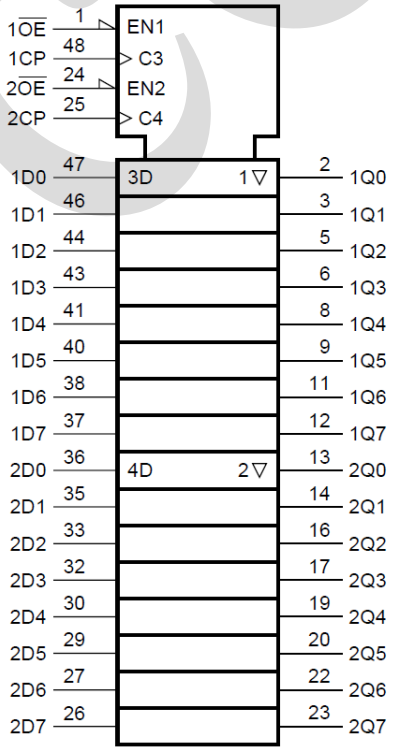


Figure 2. IEC logic symbol

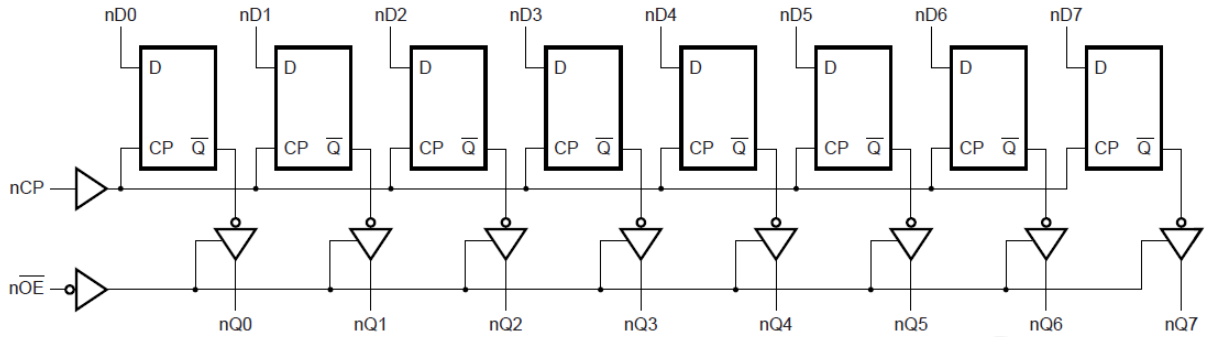
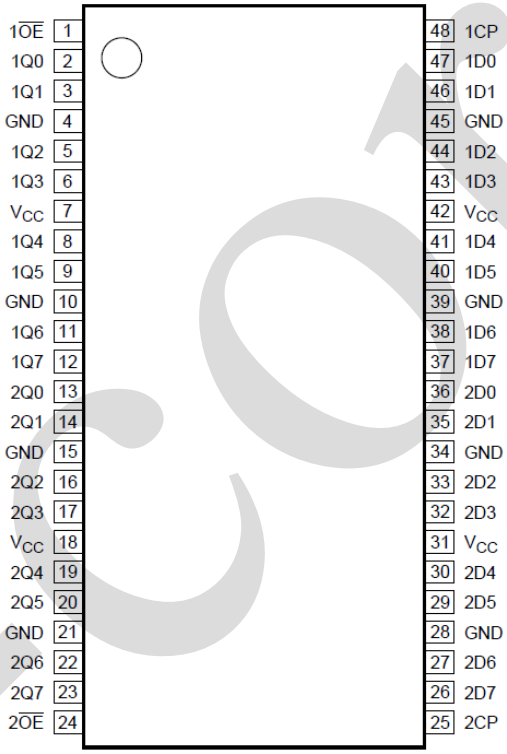


Figure 3. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1,24	$1\overline{OE}$,$2\overline{OE}$	output enable input (active LOW)
48,25	1CP,2CP	clock inputs
2,3,5,6,8,9,11,12	1Q0 to 1Q7	data outputs
13,14,16,17,19,20,22,23	2Q0 to 2Q7	data outputs
4,10,15,21,28,34,39,45	GND	ground (0V)
7,18,31,42	V_{CC}	supply voltage
47,46,44,43,41,40,38,37	1D0 to 1D7	data inputs
36,35,33,32,30,29,27,26	2D0 to 2D7	data inputs

2.4、Function Table

Operating mode	Inputs			Internal register	Output
	$n\overline{OE}$	nCP	nDn		nQ0 to nQ7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	NC	X	NC	Z
	H	↑	nDn	nDn	Z

Note:

H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;

L = LOW voltage level;

l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;

NC = no change;

X = don't care;

Z = high-impedance OFF-state;

↑ = LOW-to-HIGH clock transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+4.6	V
input voltage	V_I	-[1]	-0.5	+7.0	V
output voltage	V_O	output in OFF-state or HIGH-state[1]	-0.5	+7.0	V
input clamping current	I_{IK}	V_I<0V	-50	-	mA
output clamping current	I_{OK}	V_O<0V	-50	-	mA
output current	I_O	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
storage temperature	T_{stg}	-	-65	+150	℃
junction temperature	T_j	-[2]	-	150	℃
total power dissipation	P_{tot}	-	-	500	mW
Soldering temperature	T_L	10s	260		℃

Note:

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	-	2.7	-	3.6	V
input voltage	V_I	-	0	-	5.5	V
HIGH-level input voltage	V_{IH}	-	2.0	-	-	V
LOW-level input voltage	V_{IL}	-	-	-	0.8	V
HIGH-level output current	I_{OH}	-	-32	-	-	mA
LOW-level output current	I_{OL}	none	-	-	32	mA
		current duty cycle≤50%; f_i≥1kHz	-	-	64	mA
ambient temperature	T_{amb}	in free-air	-40	-	+125	℃
input transition rise and fall rate	Δt/ΔV	outputs enabled	-	-	10	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}=-18mA		-1.2	-0.85	-	V
HIGH-level output voltage	V_{OH}	I_{OH} =-100uA; V_{CC} =2.7V to 3.6V		V_{CC}-0.2	V_{CC}	-	V
		I_{OH}=-8mA; V_{CC}=2.7V		2.4	2.5	-	V
		I_{OH}=-32mA; V_{CC}=3.0V		2.0	2.3	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V	I_{OL}=100uA	-	0.07	0.2	V
			I_{OL}=24mA	-	0.3	0.5	V
		V_{CC}=3.0V	I_{OL}=16mA	-	0.25	0.4	V
			I_{OL}=32mA	-	0.3	0.5	V
			I_{OL} =64mA	-	0.4	0.55	V
power-up LOW-level output voltage	$V_{OL(pu)}$	V_{CC} = 3.6 V; I_O = 1 mA; V_I = V_{CC} or GND[2]		-	0.1	0.55	V
input leakage current	I_I	control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
			V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		input data pins[3]	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
			V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-5	-	-	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA

bus hold LOW current	I_{BHL}	V_{CC}=3V; V_I=0.8V		75	135	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3V; V_I=2.0V		-	-135	-75	uA
bus hold LOW overdrive current	I_{BHLO}	input data pins; V_I=0V to 3.6V; V_{CC}=3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	input data pins; V_I=0V to 3.6V; V_{CC}=3.6V[4]		-	-	-500	uA
output leakage current	I_{LO}	output in HIGH-state when V_O>V_{CC}; V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; n$\overline{OE}$ = don't care[5]		-	-	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	output HIGH: V_O=3.0V	-	-	5	uA
			output LOW: V_O=0.5V	-5	-	-	uA
supply current	I_{CC}	V_{CC}=3.6V; V_I=GND or V_{CC}; I_O=0A	outputs HIGH	-	-	0.12	mA
			outputs LOW	-	-	0.12	mA
			outputs disabled[6]	-	-	0.12	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V, other inputs at V_{CC} or GND[7]		-	-	0.2	mA
input capacitance	C_I	input pins;V_I=0V or 3.0V		-	3	-	pF
output capacitance	C_O	output pins nQn;outputs disabled; V_O=0V or V_{CC}		-	9	-	pF

Note:

[1] Typical values are measured at V_{CC}=3.3V and at T_{amb}=25℃.

[2] For valid test results, data must not be loaded into the flips-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. [1]	Max.	Unit
input clamping voltage	V_{IK}	V_{CC}=2.7V; I_{IK}=-18mA		-1.2	-	-	V
HIGH-level output voltage	V_{OH}	I_{OH} =-100uA; V_{CC} =2.7V to 3.6V		V_{CC}-0.2	-	-	V
		I_{OH}=-8mA; V_{CC}=2.7V		2.4	-	-	V
		I_{OH}=-32mA; V_{CC}=3.0V		2.0	-	-	V
LOW-level output voltage	V_{OL}	V_{CC}=2.7V	I_{OL}=100uA	-	-	0.2	V
			I_{OL}=24mA	-	-	0.5	V
		V_{CC}=3.0V	I_{OL}=16mA	-	-	0.4	V
			I_{OL}=32mA	-	-	0.5	V
			I_{OL} =64mA	-	-	0.55	V
power-up LOW-level output voltage	$V_{OL(pu)}$	V_{CC} = 3.6 V; I_O = 1 mA; V_I = V_{CC} or GND[2]		-	-	0.55	V
input leakage current	I_I	control pins	V_{CC}=3.6V; V_I=V_{CC} or GND	-	-	±1	uA
			V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
		input data pins[3]	V_{CC}=0V or 3.6V; V_I=5.5V	-	-	10	uA
			V_{CC}=3.6V; V_I=V_{CC}	-	-	1	uA
			V_{CC}=3.6V; V_I=0V	-5	-	-	uA
power-off leakage current	I_{OFF}	V_{CC}=0V; V_I or V_O=0V to 4.5V		-	-	±100	uA
bus hold LOW current	I_{BHL}	V_{CC}=3V; V_I=0.8V		75	-	-	uA
bus hold HIGH current	I_{BHH}	V_{CC}=3V; V_I=2.0V		-	-	-75	uA
bus hold LOW overdrive current	I_{BHLO}	input data pins; V_I=0V to 3.6V; V_{CC}=3.6V[4]		500	-	-	uA
bus hold HIGH overdrive current	I_{BHHO}	input data pins; V_I=0V to 3.6V; V_{CC}=3.6V[4]		-	-	-500	uA
output leakage current	I_{LO}	output in HIGH-state when V_O>V_{CC}; V_O=5.5V; V_{CC}=3.0V		-	-	125	uA
power-up/ power-down output current	$I_{O(pu/pd)}$	V_{CC}≤1.2V; V_O=0.5V to V_{CC}; V_I=GND or V_{CC}; $n\overline{OE}$ = don't care[5]		-	-	±100	uA
OFF-state output current	I_{OZ}	V_{CC}=3.6V; V_I=V_{IH} or V_{IL}	output HIGH: V_O=3.0V	-	-	5	uA
			output LOW: V_O=0.5V	-5	-	-	uA
supply current	I_{CC}	V_{CC}=3.6V;	outputs HIGH	-	-	0.12	mA

		V_I=GND or V_{CC}; I_O=0A	outputs LOW	-	-	0.12	mA
			outputs disabled[6]	-	-	0.12	mA
additional supply current	ΔI_{CC}	per input pin; V_{CC}=3.0V to 3.6V; one input at V_{CC}-0.6V, other inputs at V_{CC} or GND[7]		-	-	0.2	mA

Note:

[1] Typical values are measured at V_{CC}=3.3V and at T_{amb}=25℃.

[2] For valid test results, data must not be loaded into the flips-flops (or latches) after applying power.

[3] Unused pins at V_{CC} or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10ms. From V_{CC}=1.2V to V_{CC}=3.3V±0.3V a transition time of 100us is permitted. This parameter is valid for T_{amb}=25℃ only.

[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

3.3.3、AC Characteristics 1

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
maximum frequency	f_{max}	nCP; V_{CC}=3.3V±0.3V; see Figure 4		150	-	-	MHz
LOW to HIGH propagation delay	t_{PLH}	nCP to nQn; see Figure 4	V_{CC}=3.3V±0.3V	1.5	4.1	7.0	ns
			V_{CC}=2.7V	-	-	7.8	ns
HIGH to LOW propagation delay	t_{PHL}	nCP to nQn; see Figure 4	V_{CC}=3.3V±0.3V	1.5	4.2	7.0	ns
			V_{CC}=2.7V	-	-	7.8	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V±0.3V	1.5	4.5	6.7	ns
			V_{CC}=2.7V	-	-	8.4	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V±0.3V	1.5	4.2	6.4	ns
			V_{CC}=2.7V	-	-	7.3	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V±0.3V	1.5	5.5	7.6	ns
			V_{CC}=2.7V	-	-	8.4	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V±0.3V	1.5	4.8	6.4	ns
			V_{CC}=2.7V	-	-	7.0	ns
set-up time	t_{su}	nDn to nCP; HIGH or LOW; see Figure 6[2]	V_{CC}=3.3V±0.3V	2.0	1.0	-	ns
			V_{CC}=2.7V	2.0	-	-	ns
hold time	t_h	nDn to nCP; HIGH or LOW; see Figure 6[3]	V_{CC}=3.3V±0.3V	0.8	0.0	-	ns
			V_{CC}=2.7V	0.1	-	-	ns
pulse width	t_W	nCP HIGH; see Figure 4[4]	V_{CC}=3.3V±0.3V	1.5	0.8	-	ns
			V_{CC}=2.7V	1.5	-	-	ns
		nCP LOW;	V_{CC}=3.3V±0.3V	3.0	2.2		ns

		see Figure 4	V_{CC}=2.7V	3.0	-	-	ns

Note:

[1] All typical values are at V_{CC}=3.3V and T_{amb}=25℃.

[2] t_{su} is the same as $t_{su(H)}$ and $t_{su(L)}$.

[3] t_h is the same as $t_{h(H)}$ and $t_{h(L)}$.

[4] t_W is the same as $t_{W(H)}$ and $t_{W(L)}$.

3.3.4、AC Characteristics 2

(T_{amb}=-40℃ to +125℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.[1]	Max.	Unit
maximum frequency	f_{max}	nCP; V_{CC}=3.3V ±0.3V; see Figure 4		180	-	-	MHz
LOW to HIGH propagation delay	t_{PLH}	nCP to nQn; see Figure 4	V_{CC}=3.3V ±0.3V	1.8	-	8.4	ns
			V_{CC}=2.7V	-	-	9.4	ns
HIGH to LOW propagation delay	t_{PHL}	nCP to nQn; see Figure 4	V_{CC}=3.3V ±0.3V	1.8	-	8.4	ns
			V_{CC}=2.7V	-	-	9.4	ns
OFF-state to HIGH propagation delay	t_{PZH}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V ±0.3V	1.8	-	8.1	ns
			V_{CC}=2.7V	-	-	10.1	ns
OFF-state to LOW propagation delay	t_{PZL}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V ±0.3V	1.8	-	7.7	ns
			V_{CC}=2.7V	-	-	8.7	ns
HIGH to OFF-state propagation delay	t_{PHZ}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V ±0.3V	1.8	-	9.1	ns
			V_{CC}=2.7V	-	-	10.1	ns
LOW to OFF-state propagation delay	t_{PLZ}	n$\overline{OE}$ to nQn; see Figure 5	V_{CC}=3.3V ±0.3V	1.8	-	7.7	ns
			V_{CC}=2.7V	-	-	8.4	ns
set-up time	t_{su}	nDn to nCP; HIGH or LOW; see Figure 6[2]	V_{CC}=3.3V ±0.3V	2.4	-	-	ns
			V_{CC}=2.7V	2.4	-	-	ns
hold time	t_h	nDn to nCP; HIGH or LOW; see Figure 6[3]	V_{CC}=3.3V ±0.3V	1.0	-	-	ns
			V_{CC}=2.7V	0.1	-	-	ns
pulse width	t_W	nCP HIGH; see Figure 4[4]	V_{CC}=3.3V ±0.3V	1.8	-	-	ns
			V_{CC}=2.7V	1.8	-	-	ns
		nCP LOW; see Figure 4	V_{CC}=3.3V ±0.3V	3.6	-	-	ns
			V_{CC}=2.7V	3.6	-	-	ns

Note:

[1] All typical values are at V_{CC}=3.3V and T_{amb}=25℃.

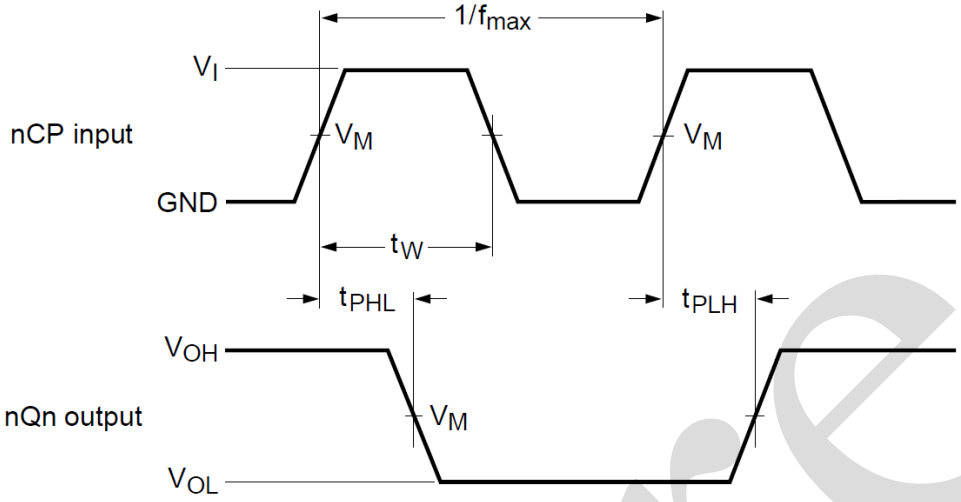
[2] t_{su} is the same as $t_{su(H)}$ and $t_{su(L)}$.

[3] t_h is the same as $t_{h(H)}$ and $t_{h(L)}$.

[4] t_W is the same as $t_{W(H)}$ and $t_{W(L)}$.

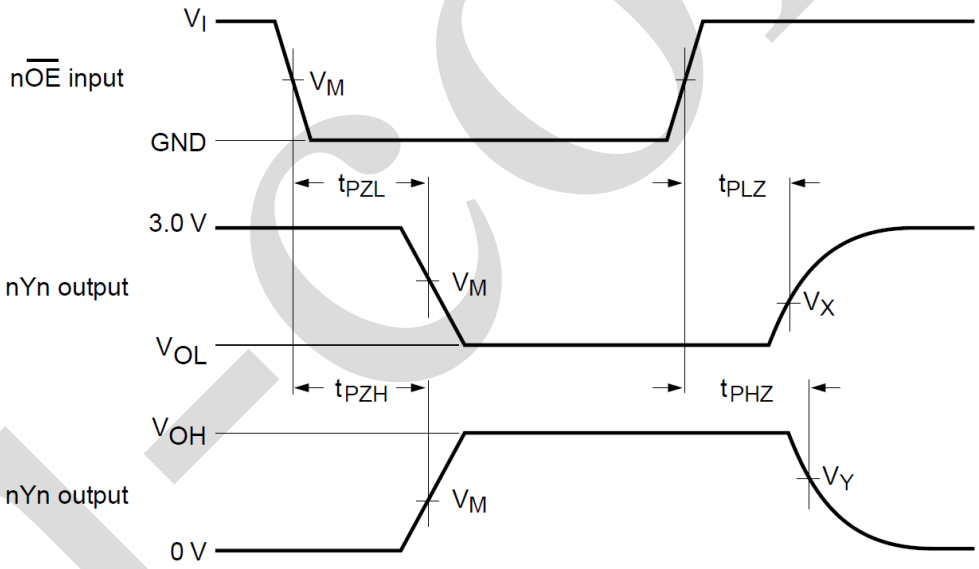
4、Testing Circuit

4.1、AC Testing Waveforms



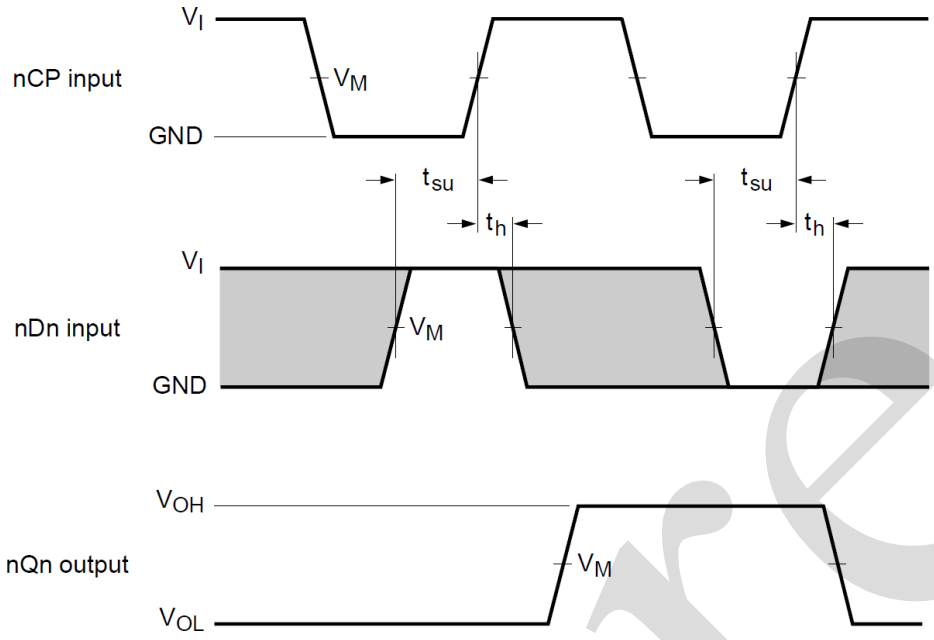
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 4. Propagation delay clock input to output, clock pulse width and maximum clock frequency



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Enable and disable times



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Remark: The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 6. Data set-up and hold times

4.2、Measurement Points

Input	Output		
V_M	**V_M**	**V_X**	**V_Y**
1.5V	1.5V	V_{OL}+0.3V	V_{OH}-0.3V

4.3、AC Testing Circuit

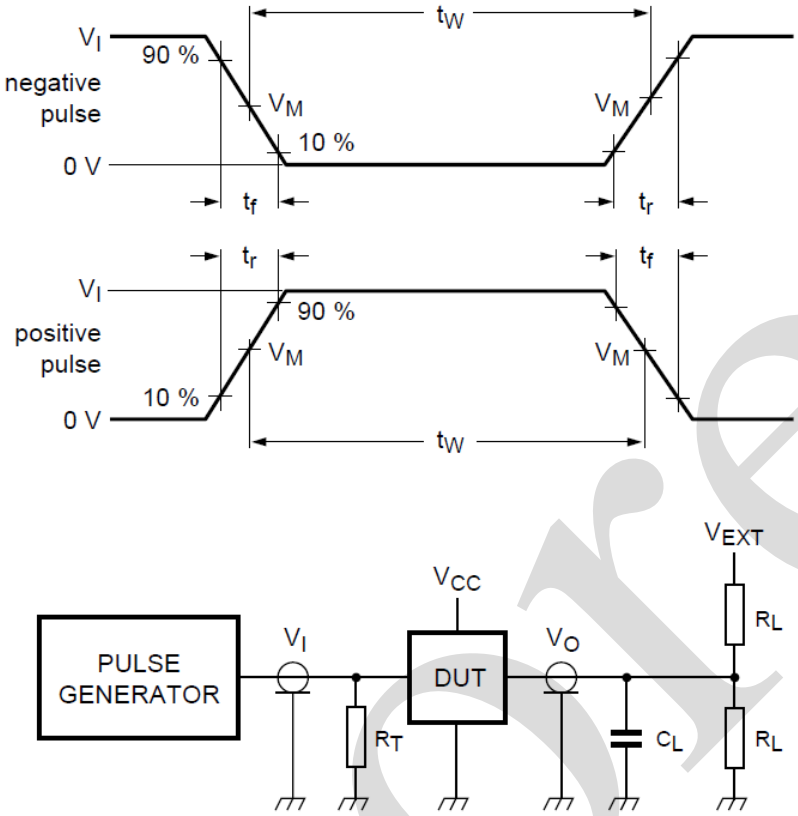


Figure 6. Test circuit for measuring switching times

Definitions test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to output impedance Z_o of the pulse generator.

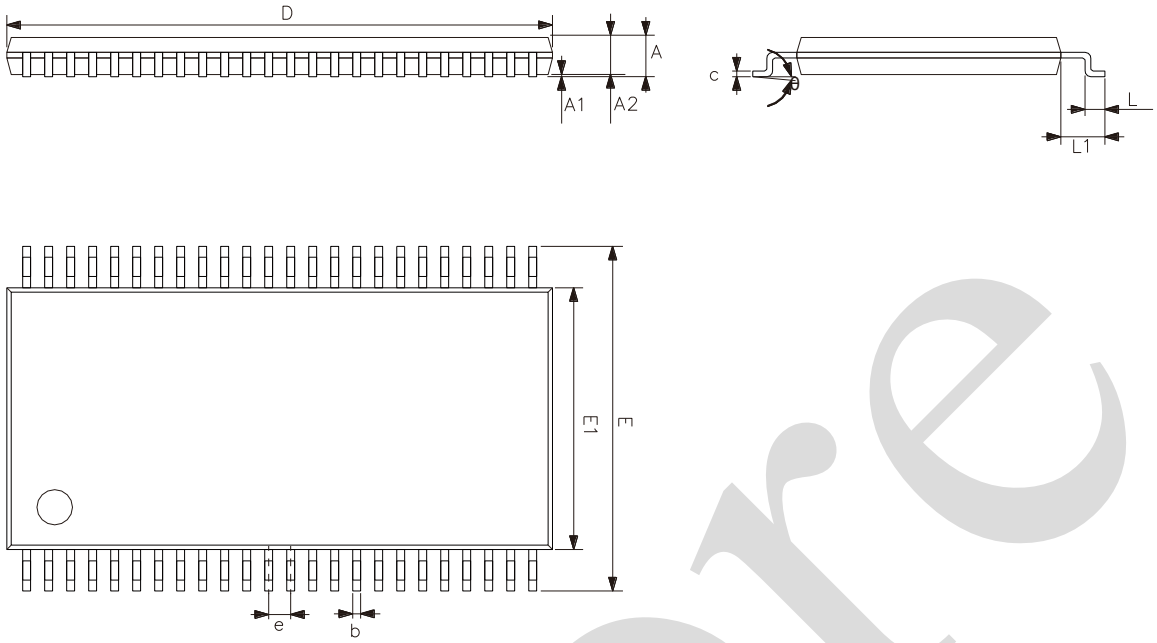
V_{EXT}=Test voltage for switching times.

4.4、Test Data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r , t_f	C_L	R_L	t_{PHZ} , t_{PZH}	t_{PLZ} , t_{PZL}	t_{PLH} , t_{PHL}
2.7V	≤10MHz	500ns	≤2.5ns	50pF	500Ω	GND	6V	open

5、Package Information

5.1、TSSOP48



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.03	0.15
A2	0.82	1.05
b	0.17	0.27
c	0.12	0.22
D	12.40	12.60
E	7.90	8.30
E1	6.00	6.20
e	0.50	
L	0.35	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core's application to avoid failure in the application or the application of the customer' s third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form i-Core's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.