



CD4051H

8-channel Analog Multiplexer/Demultiplexer

Product Specification

Specification Revision History:

Version	Date	Description
2021-11-A1	2021-11	New
2023-04-B1	2023-04	Update the template



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1、General Description

The CD4051H is an 8-channel analog multiplexer/demultiplexer with three address inputs (S1 to S3), an active LOW enable input ($\bar{E}$), eight independent inputs/outputs (Y0 to Y7) and a common input/output (Z). The device contains eight bidirectional analog switches, each with one side connected to an independent input/output (Y0 to Y7) and the other side connected to a common input/output (Z). With $\bar{E}$ LOW, one of the eight switches is selected (low-impedance ON-state) by S1 to S3. With $\bar{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. If break before make is needed, then it is necessary to use the enable input.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S1 to S3, and $\bar{E}$). The V_{DD} to V_{SS} range is 3V to 18V. The analog inputs/outputs (Y0 to Y7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD}-V_{EE}$ may not exceed 18V. Unused inputs must be connected to V_{DD} , V_{SS} , or another input. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground). V_{EE} and V_{SS} are the supply voltage connections for the switches.

Features:

- Wide supply voltage range from 3V to 18V
- Fully static operation
- 5V, 10V and 18V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16/DHVQFN16

**Ordering Information:****Tube packing specifications:**

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4051HDA16.TB	DIP16	CD4051H	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4051HSA16.TB	SOP16	CD4051H	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing: 1.27mm
CD4051HTA16.TB	TSSOP16	CD4051H	96 PCS/tube	200 tube/box	19200 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4051HSA16.TR	SOP16	CD4051H	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4051HTA16.TR	TSSOP16	CD4051H	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
CD4051HQE16.TR	DHVQFN16	CD4051H	3000 PCS/reel	3000 PCS/box	Dimensions of plastic enclosure: 3.5mm×2.5mm Pin spacing: 0.5mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.



2、Block Diagram And Pin Description

2.1、Block Diagram

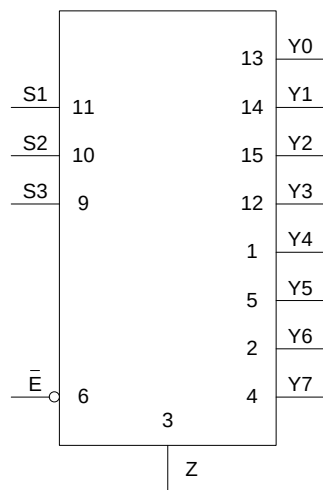


Figure 1. Logic symbol

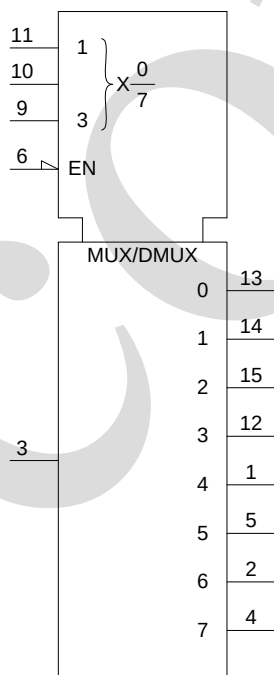


Figure 2. IEC logic symbol

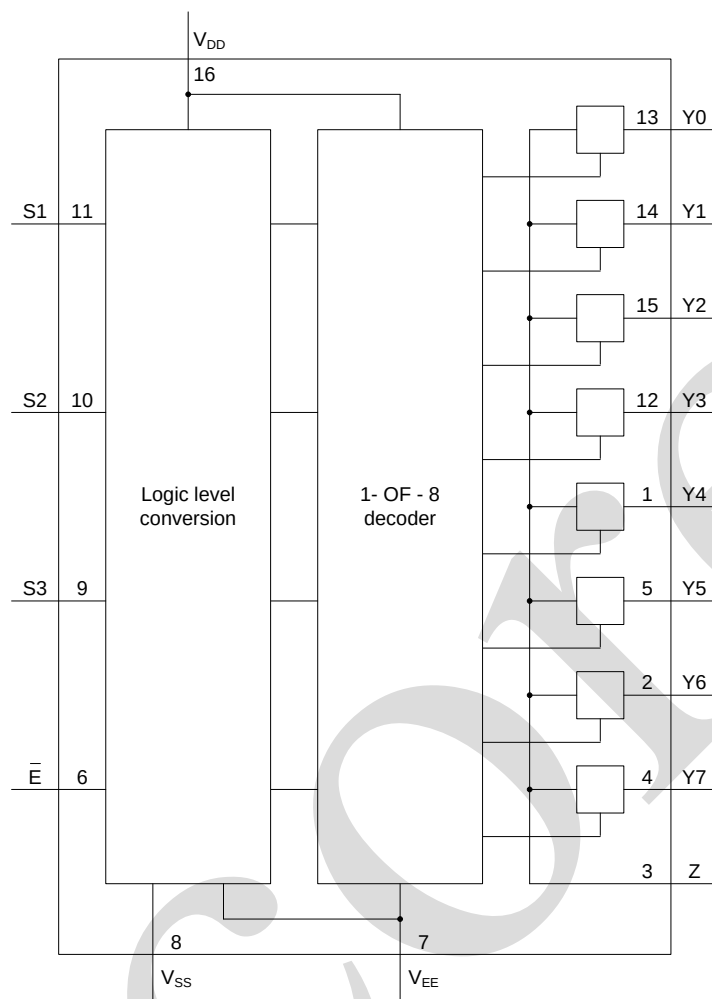


Figure 3. Functional diagram

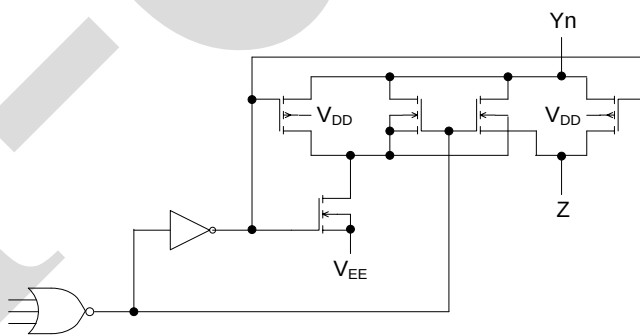


Figure 4. Schematic diagram (one switch)

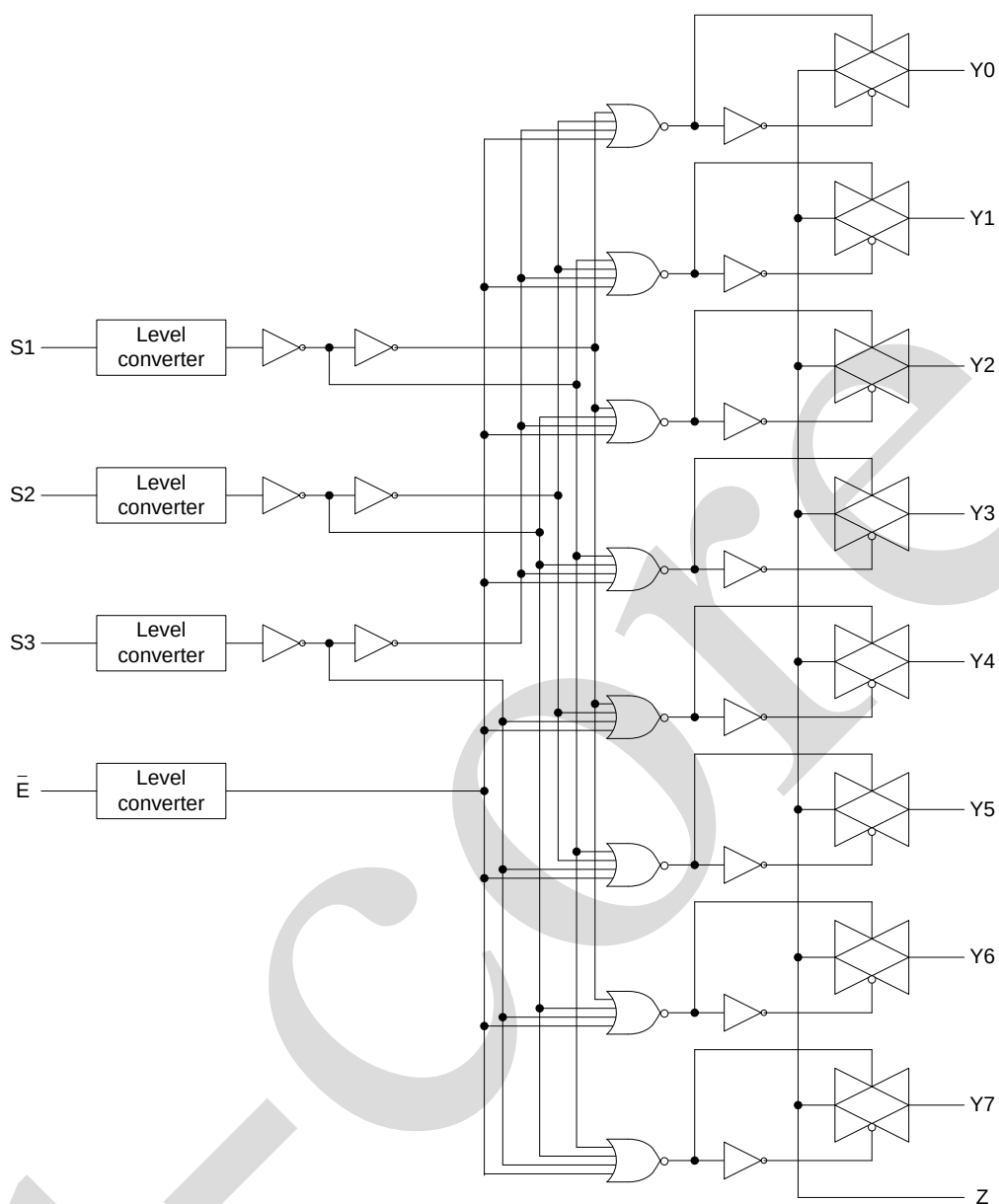
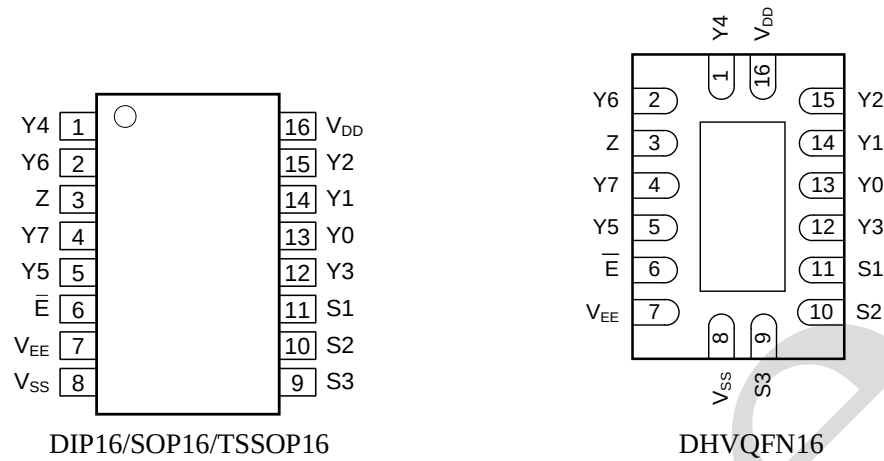


Figure 5. Logic diagram



2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	Y4	independent input or output
2	Y6	independent input or output
3	Z	common output or input
4	Y7	independent input or output
5	Y5	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V_{EE}	supply voltage
8	V_{SS}	ground (0V)
9	S3	select input
10	S2	select input
11	S1	select input
12	Y3	independent input or output
13	Y0	independent input or output
14	Y1	independent input or output
15	Y2	independent input or output
16	V_{DD}	supply voltage



2.4、Function Table

Input				Channel ON
$\bar{E}$	S3	S2	S1	
L	L	L	L	Y0 to Z
L	L	L	H	Y1 to Z
L	L	H	L	Y2 to Z
L	L	H	H	Y3 to Z
L	H	L	L	Y4 to Z
L	H	L	H	Y5 to Z
L	H	H	L	Y6 to Z
L	H	H	H	Y7 to Z
H	X	X	X	switches off

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{DD}	-	-0.5	+21	V
supply voltage	V_{EE}	-	-21	+0.5	V
input voltage	V_I	-	-0.5	$V_{DD}+0.5$	V
input clamping current	I_{IK}	$V_I < 0.5V$ or $V_I > V_{DD}+0.5V$	-	± 10	mA
Input/output current	$I_{I/O}$	-	-	± 10	mA
supply current	I_{DD}	-	-	50	mA
storage temperature	T_{stg}	-	-65	+150	°C
ambient temperature	T_{amb}	-	-40	+125	°C
total power dissipation	P_{tot}	-	-	500	mW
device dissipation	P	per output transistor	-	100	mW
soldering temperature	T_L	10s	DIP	245	°C
			SOP/TSSOP/DHVQFN	260	°C

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	18	V
supply voltage	V_{EE}	-	-15	-	0	V
supply voltage	$V_{DD}-V_{EE}$	-	3	-	18	V
input voltage	V_I	-	0	-	V_{DD}	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{DD}=5V$	-	-	3.75	us/V
		$V_{DD}=10V$	-	-	0.5	us/V
		$V_{DD}=18V$	-	-	0.08	us/V

**3.3、Electrical Characteristics****3.3.1、DC Characteristics 1**(T_{amb}=25℃, V_{SS}=V_{EE}=0V; V_I=V_{SS} or V_{DD}, I_{SW}=200uA, unless otherwise specified.)

Parameter	Symbol	Conditions (V)		T _{amb} =25℃			Unit
				Min.	Typ.	Max.	
HIGH-level input voltage	V _{IH}	I _O <1uA	V _{DD} =5V	3.5	-	-	V
			V _{DD} =10V	7.0	-	-	V
			V _{DD} =18V	12.6	-	-	V
LOW-level input voltage	V _{IL}	I _O <1uA	V _{DD} =5V	-	-	1.5	V
			V _{DD} =10V	-	-	3.0	V
			V _{DD} =18V	-	-	5.4	V
supply current	I _{DD}	I _O =0A	V _{DD} =5V	-	-	5	uA
			V _{DD} =10V	-	-	10	uA
			V _{DD} =18V	-	-	20	uA
input leakage current	I _I	V _{DD} =18V		-	-	±1.0	uA
OFF-state leakage current	I _{S(OFF)}	V _{DD} =18V	Z port; all channels OFF; see Figure 6	-	-	±1.0	uA
			Y port; per channel; see Figure 7	-	-	±1.0	uA
ON resistance (peak)	R _{ON(peak)}	V _I =0V to V _{DD} -V _{EE} ; see Figure 8 and Figure 9	V _{DD} -V _{EE} =5V	-	117	836	Ω
			V _{DD} -V _{EE} =10V	-	58	178	Ω
			V _{DD} -V _{EE} =15V	-	41	120	Ω
			V _{DD} -V _{EE} =20V	-	36	105	Ω
ON resistance (rail)	R _{ON(rail)}	V _I =0V; see Figure 8 and Figure 9	V _{DD} -V _{EE} =5V	-	44	130	Ω
			V _{DD} -V _{EE} =10V	-	29	93	Ω
			V _{DD} -V _{EE} =15V	-	24	69	Ω
			V _{DD} -V _{EE} =20V	-	22	63	Ω
		V _I =V _{DD} -V _{EE} ; see Figure 8 and Figure 9	V _{DD} -V _{EE} =5V	-	82	249	Ω
			V _{DD} -V _{EE} =10V	-	51	157	Ω
			V _{DD} -V _{EE} =15V	-	41	127	Ω
			V _{DD} -V _{EE} =20V	-	36	112	Ω
ON resistance mismatch between channels	ΔR _{ON}	V _I =0V to V _{DD} -V _{EE} ; see Figure 8	V _{DD} -V _{EE} =5V	-	25	-	Ω
			V _{DD} -V _{EE} =10V	-	10	-	Ω
			V _{DD} -V _{EE} =15V	-	5	-	Ω
			V _{DD} -V _{EE} =20V	-	5	-	Ω
input capacitance	C _I	Sn, $\bar{E}$ inputs		-	-	7.5	pF



3.3.2、DC Characteristics 2

($T_{amb}=-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{SS}=V_{EE}=0\text{V}$; $V_I=V_{SS}$ or V_{DD} , unless otherwise specified.)

Parameter	Symbol	Conditions (V)	$T_{amb}=-40^{\circ}\text{C}$		$T_{amb}=+85^{\circ}\text{C}$		$T_{amb}=+125^{\circ}\text{C}$		Unit
			Min.	Min.	Min.	Max.	Min.	Max.	
HIGH-level input voltage	V_{IH}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	3.5	-	3.5	-	3.5	V
			$V_{DD}=10\text{V}$	7.0	-	7.0	-	7.0	V
			$V_{DD}=18\text{V}$	12.6	-	12.6	-	12.6	V
LOW-level input voltage	V_{IL}	$ I_O <1\mu\text{A}$	$V_{DD}=5\text{V}$	-	1.5	-	1.5	-	V
			$V_{DD}=10\text{V}$	-	3.0	-	3.0	-	V
			$V_{DD}=18\text{V}$	-	5.4	-	5.4	-	V
supply current	I_{DD}	$I_O=0\text{A}$	$V_{DD}=5\text{V}$	-	5	-	150	-	μA
			$V_{DD}=10\text{V}$	-	10	-	300	-	μA
			$V_{DD}=18\text{V}$	-	20	-	600	-	μA
input leakage current	I_I	$V_{DD}=18\text{V}$	-	± 1.0	-	± 1.0	-	± 1.0	μA

3.3.3、AC Characteristics 1

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay time	t_{PHL}	Yn to Z; Z to Yn; see Figure 11	$V_{DD}=5\text{V}$	-	15	ns
			$V_{DD}=10\text{V}$	-	5	ns
			$V_{DD}=18\text{V}$	-	5	ns
		Sn to Yn, Z; see Figure 12	$V_{DD}=5\text{V}$	-	150	ns
			$V_{DD}=10\text{V}$	-	60	ns
			$V_{DD}=18\text{V}$	-	45	ns
LOW to HIGH propagation delay	t_{PLH}	Yn to Z; Z to Yn; see Figure 11	$V_{DD}=5\text{V}$	-	15	ns
			$V_{DD}=10\text{V}$	-	5	ns
			$V_{DD}=18\text{V}$	-	5	ns
		Sn to Yn, Z; see Figure 12	$V_{DD}=5\text{V}$	-	150	ns
			$V_{DD}=10\text{V}$	-	65	ns
			$V_{DD}=18\text{V}$	-	45	ns
HIGH to OFF-state propagation delay	t_{PHZ}	$\bar{E}$ to Yn, Z; see Figure 13	$V_{DD}=5\text{V}$	-	120	ns
			$V_{DD}=10\text{V}$	-	90	ns
			$V_{DD}=18\text{V}$	-	85	ns
LOW to OFF-state propagation delay	t_{PLZ}	$\bar{E}$ to Yn, Z; see Figure 13	$V_{DD}=5\text{V}$	-	145	ns
			$V_{DD}=10\text{V}$	-	120	ns
			$V_{DD}=18\text{V}$	-	115	ns
OFF-state to HIGH propagation delay	t_{PZH}	$\bar{E}$ to Yn, Z; see Figure 13	$V_{DD}=5\text{V}$	-	140	ns
			$V_{DD}=10\text{V}$	-	55	ns
			$V_{DD}=18\text{V}$	-	40	ns
OFF-state to LOW propagation delay	t_{PZL}	$\bar{E}$ to Yn, Z; see Figure 13	$V_{DD}=5\text{V}$	-	140	ns
			$V_{DD}=10\text{V}$	-	55	ns
			$V_{DD}=18\text{V}$	-	40	ns



3.3.4、AC Characteristics 2

($T_{amb}=25^{\circ}\text{C}$, $V_{EE}=V_{SS}=0\text{V}$, $V_I=0.5V_{DD}$ (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
total harmonic distortion	THD	see Figure 14; R _L =10 kΩ; C _L =15pF; channel ON; f _i =1kHz	V _{DD} =5V	-	0.25	-	%
			V _{DD} =10V	-	0.04	-	%
			V _{DD} =18V	-	0.04	-	%
-3dB frequency response	f _(-3dB)	see Figure 15; R _L =1kΩ; C _L =5pF; channel ON;	V _{DD} =5V	-	13	-	MHz
			V _{DD} =10V	-	40	-	MHz
			V _{DD} =18V	-	70	-	MHz
isolation (OFF-state)	α _{iso}	see Figure 16; f _i =1MHz; R _L =1kΩ; C _L =5pF; channel OFF; V _{DD} =10V		-	-50	-	dB
crosstalk voltage	V _{ct}	digital inputs to switch; see Figure 17; R _L =10kΩ; C _L =15pF; $\bar{E}$ or Sn=V _{DD} (square-wave); V _{DD} =10V		-	50	-	mV
crosstalk	Xtalk	between switches; see Figure 18; f _i =1MHz; R _L =1kΩ; V _{DD} =10V		-	-50	-	dB

Note:

[1] f_i is biased at $0.5V_{DD}$; $V_I=0.5V_{DD}$ (p-p).

4、Testing Circuit

4.1、DC Testing Circuit

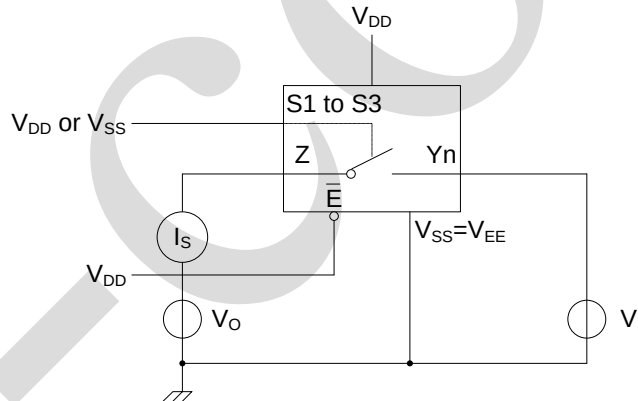


Figure 6. Test circuit for measuring OFF-state leakage current Z port

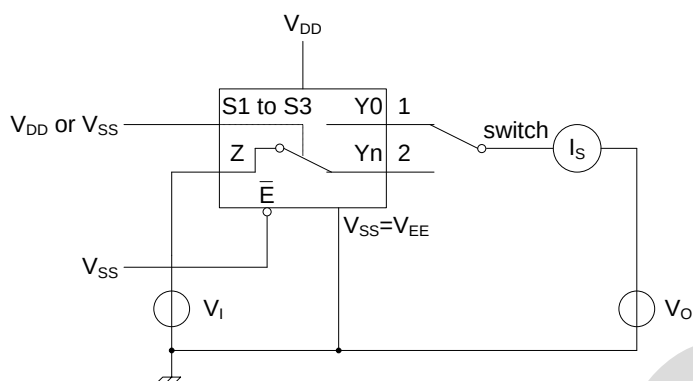


Figure 7. Test circuit for measuring OFF-state leakage current Yn port

4.2、ON resistance Testing Circuit

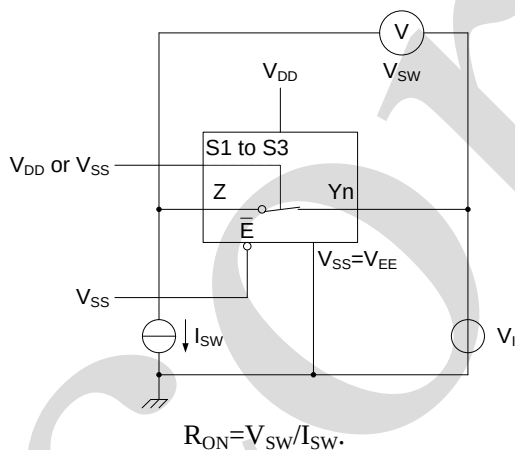


Figure 8. Test circuit for measuring R_{ON}

4.3、ON resistance Waveforms

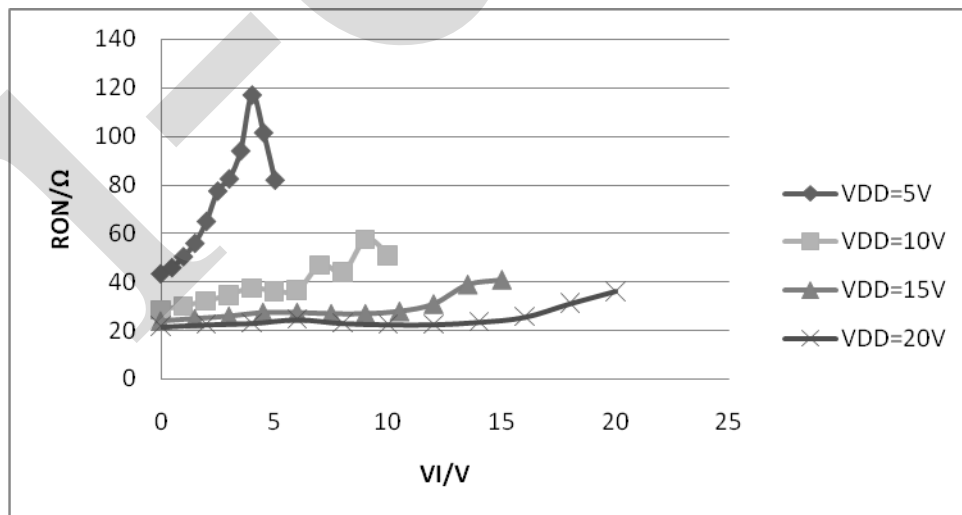


Figure 9. Typical R_{ON} as a function of input voltage



4.4、AC Testing Circuit 1

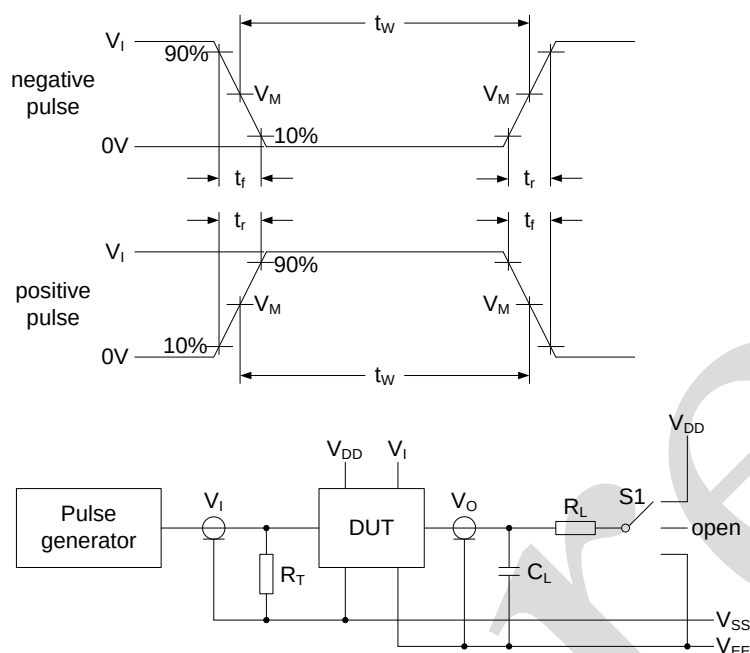


Figure 10. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance.

4.5、AC Testing Waveforms

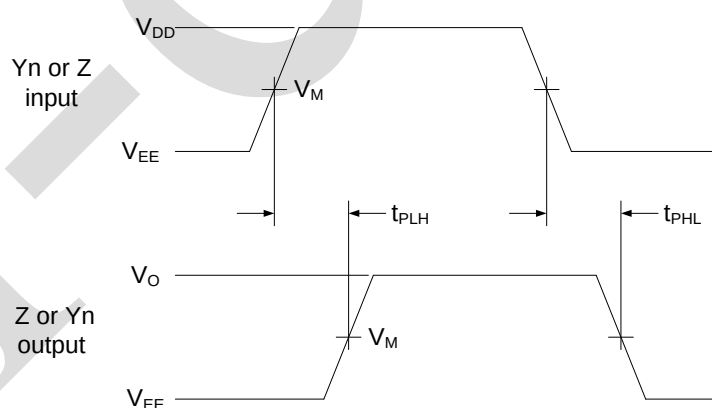


Figure 11. Yn, Z to Z, Yn propagation delays

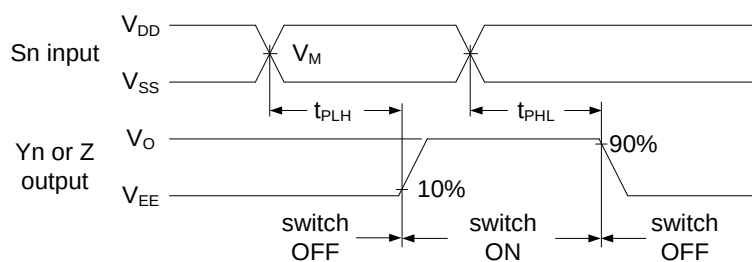


Figure 12. Sn to Yn, Z propagation delays

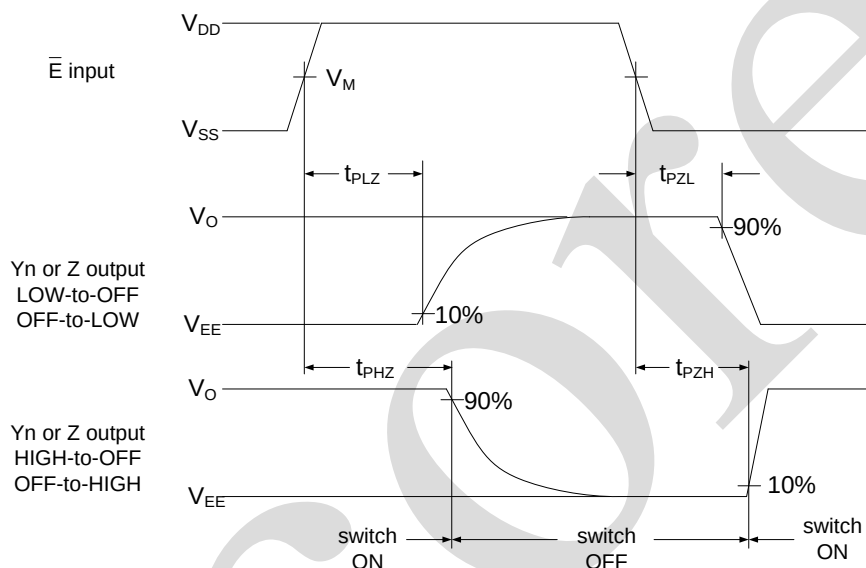


Figure 13. Enable and disable times

4.6、AC Testing Circuit 2

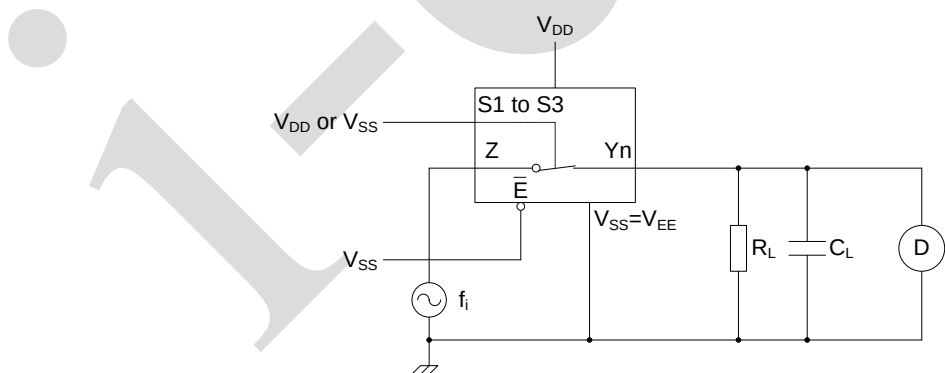


Figure 14. Test circuit for measuring total harmonic distortion

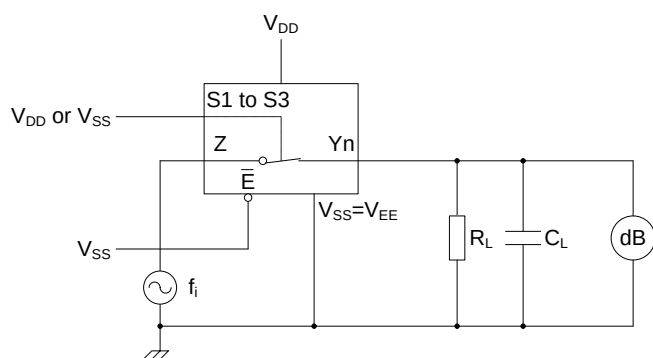


Figure 15. Test circuit for measuring frequency response

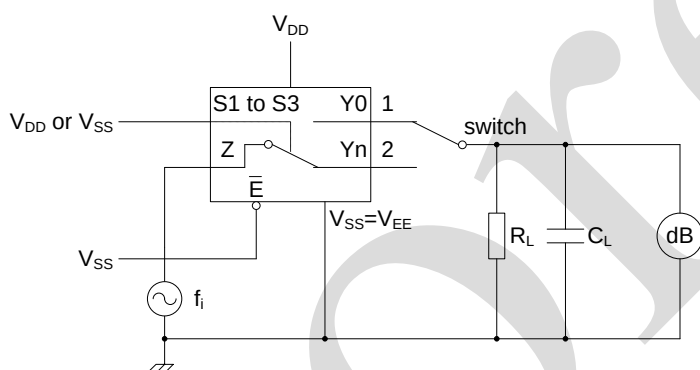
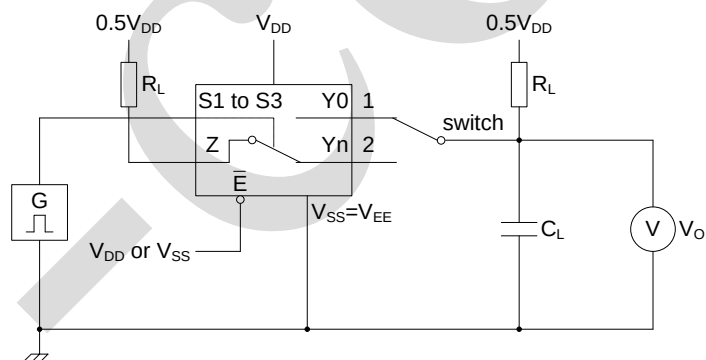
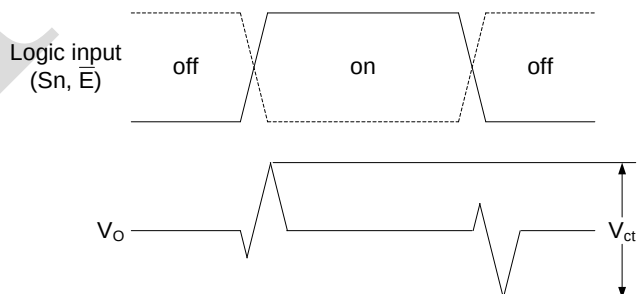


Figure 16. Test circuit for measuring isolation (OFF-state)



a. Test circuit



b. Input and output pulse definitions

Figure 17. Test circuit for measuring crosstalk voltage between digital inputs and switch



Figure 18. Test circuit for measuring crosstalk between switches

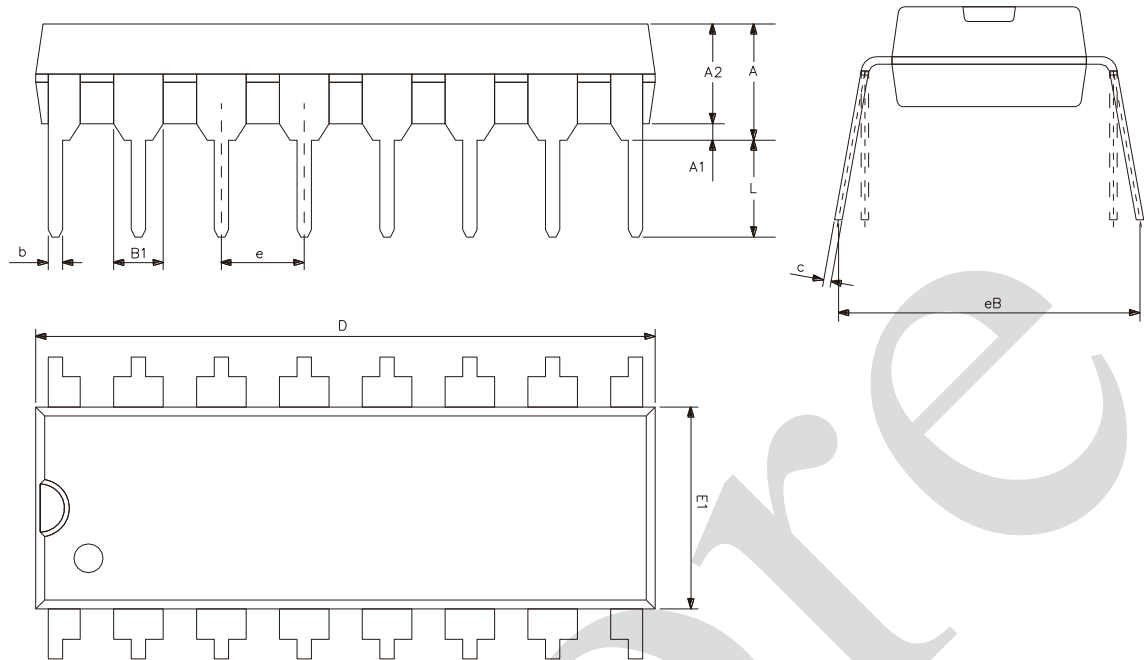
Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 18V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

Input				Load		S1 position				
Yn, Z	Sn and $\bar{E}$	t _p , t _f	V _M	C _L	R _L	t _{PHL} ^[1]	t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	other
V _{DD} or V _{EE}	V _{DD} or V _{SS}	≤20ns	0.5 × V _{DD}	50pF	10kΩ	V _{DD} or V _{EE}	V _{EE}	V _{EE}	V _{DD}	V _{EE}



5、Package Information

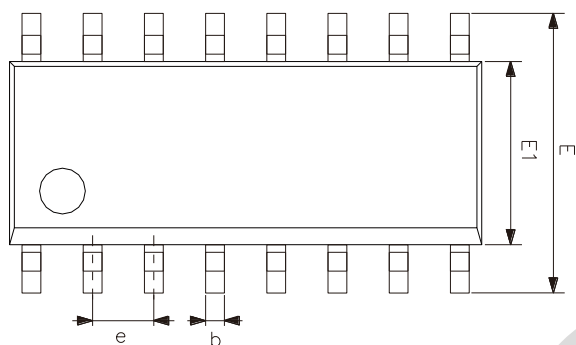
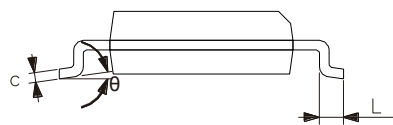
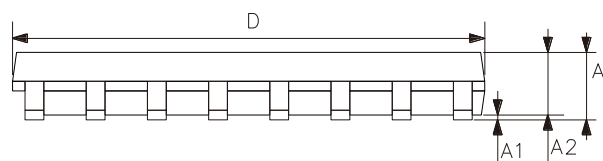
5.1、DIP16



Symbol	Dimensions (mm)	
	Min.	Max.
A2	3.20	3.60
A1	0.51	-
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



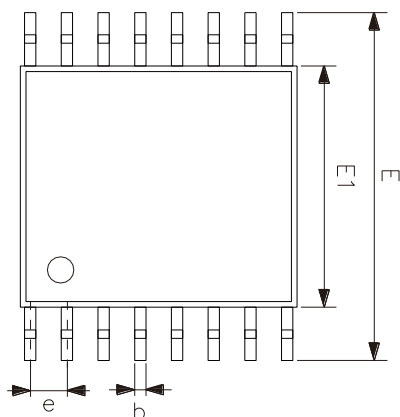
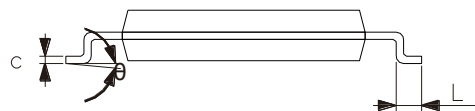
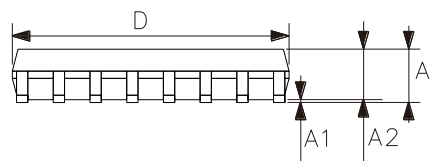
5.2、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



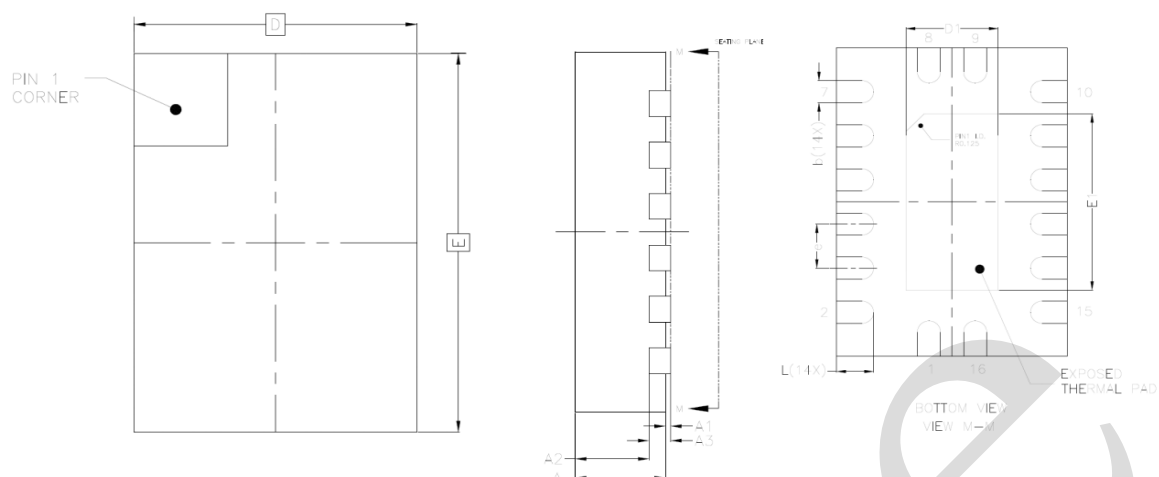
5.3、TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
θ	0°	8°



5.4、DHVQFN16



Symbol	Dimensions (mm)	
	Min.	Max.
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.70
A3	0.20	
D	2.40	2.60
E	3.40	3.60
e	0.50	
b	0.18	0.30
L	0.30	0.50
D1	0.85	1.15
E1	1.85	2.15



6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

We Recommend you to read this chapter carefully before using this product.

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